Smart Mobility ARChitecture

Hardware Specification

SMARC 2.2 Specification 2024-06-12

1 INTRODUCTION

1.1 Legal

1.2 Revision History

Rev	Date	Originator	Notes
1.0	Dec. 20, 2012	S. Milnor	Initial release
1.1	May 29, 2014	S. Milnor	Change notes for V1.0 to V1.1 can be found in the V1.1 document
2.0	June 2, 2016	C. Eder	See section 9.1 ‘Changes V1.1 to V2.0’ on page 95
2.1	March 23, 2020	C. Eder	See section 9.2 ‘Changes V2.0 to V2.1’ on page 96
2.1.1	May 20, 2020	C. Eder	Removed wrong AC coupling comment in Table 8: Secondary HDMI Signals in section 3.5.1 HDMI
2.2	June 12, 2024	S. Yagci	See section 9.4 ‘Changes V2.1.1 to V2.2’ on page 97

Table 1: Revision History

1.3 Table of Contents

1 Introduction 2
1.1 Legal 2
1.2 Revision History 2
1.3 Table of Contents 3
1.4 List of Figures 5
1.5 List of Tables 6
1.6 General Introduction 7
1.7 Purpose of This Document 7
1.8 Document and Standards References 8
2 Module Overview 10
2.1 Form Factor Feature Summary 10
2.2 Module Interface Summary 11
3 Module Interface Required and Optional Features 14
3.1 Required and Optional Feature Table 14
3.2 Feature Fill Order 16
3.3 Signal Direction and Type Definitions 17
3.4 Primary Display Interfaces 18
3.4.1 LVDS 19
3.4.2 eDP 21
3.4.3 MIPI DSI Display 23
3.4.4 LVDS / eDP / MIPI DSI Pin Sharing 24
3.5 Secondary Display Interface 25
3.5.1 HDMI 25
3.5.2 DP++ 26
3.5.3 Secondary HDMI / DP++ Pin Sharing 27
3.6 Third Display Interface 28
3.6.1 DP++ 28
3.7 Camera Interfaces 29
3.7.1 1st and 2nd MIPI CSI on SMARC Edge Connector 29
3.7.2 3rd and 4th MIPI CSI on optional feature connector 31
3.8 SDIO Card (4 bit) Interface 34
3.9 SPI Interfaces 35
3.9.1 SPI0 35
3.9.2 SPI1 35
3.9.3 QSPI 36
3.9.4 eSPI 37
3.9.5 eSPI/SPI1/QSPI Pin Sharing 38
3.10 Audio 39
3.10.1 I2S0 39
3.10.2 I2S2 40
3.10.3 HDA 40
3.10.4 Soundwire 41
3.10.5 I2S/HDA/SNDW Pin Sharing 41
3.11 I2C Interfaces 42
3.12 Asynchronous Serial Ports 43
3.13 CAN Bus 44
3.14 USB Interfaces 45
3.14.1 USB Signal Assignments 45
3.14.2 USB configurations 46
3.14.3 USB Signals 47
3.14.4 USB[0:5]_EN_OC# Discussion 49
3.15 PCI Express 50
3.15.1 PCI Express Link Width 52
3.16 SERDES 53
3.16.1 PCI Express SERDES Pin Sharing 54
3.17 SATA 55
3.18 Ethernet 56
3.19 Watchdog 58
3.20 GPIO 59
3.20.1 Alternative GPIO Pin Usage 60
3.20.2 GPIO Pin Sharing 60
3.21 Management Pins 61
3.22 Boot Select 63
3.23 Power and GND 65
3.24 JTAG 66
3.25 Module Terminations 67
3.25.1 General 67
4 Module Pin-Out Map 68
4.1 Module Pin-Out 68
5 Mechanical Definitions 73

5.1 Carrier Connector 73
5.2 Connector Pin Numbering Convention 74
5.3 Module Outline – 82x50mm Module 75
5.4 Module Outline – 82x80mm Module 76
5.4.1 RF Connector Placement 77
5.5 Module 'Z' Height Considerations 78
5.6 Carrier Board Connector PCB Footprint 79
5.7 GND Connection Mounting Holes 80
5.8 Carrier Board Standoffs 80
5.9 Thermal Attachment Points 80
5.10 Heat Spreader – 82mm x 50mm Module 81
5.11 Heat Spreader – 82mm x 80mm Module 84
5.12 Mechanical Tolerances 85
6 Module Power 86
6.1 Input Voltage / Main Power Rail 86
6.2 No Separate Standby Voltage 86
6.3 RTC Voltage Rail 86
6.4 Power Rail Definition 87
6.5 Power Sequencing 88
6.5.1 Power up sequence scenario 1 88
6.5.2 Power up sequence scenario 2 89
6.5.3 Power up sequence scenario 3 90
6.5.4 Power up sequence scenario 4 91
7 MODULE AND CARRIER SERIAL EEPROMS 92
8 Appendix A: LVDS LCD Color Mappings 93
8.1 LVDS LCD Color Mappings 93
8.1.1 Single Channel Color Mapping 94
9 Appendix B: Document Changes 95
9.1 Changes V1.1 to V2.0 95
9.2 Changes V2.0 to V2.1 96
9.3 Changes V2.1 to V2.1.1 96
9.4 Changes V2.1.1 to V2.2 97
9.5 Pinout Comparison 97
9.6 Signal Name Index 106

1.4 List of Figures

Figure 1: MIPI CSI feature connector placement (82x50mm Module) _ 33
Figure 2: MIPI CSI feature connector placement (82x80mm Module) _ 33
Figure 3: JTAG Connector _____ 66
Figure 4: 82x50mm Module Outline _____ 75
Figure 5: Module Edge Finger Keep Out Area (82x50mm Module) ___ 76
Figure 6: 82x80mm Module Outline _____ 76
Figure 7: Module Edge Finger Keep Out Area (82x80mm Module) ___ 76
Figure 8: u.FL connector _____ 77
Figure 9: RF connector placement (82x80mm Module) _____ 77
Figure 10: RF connector placement (82x50mm Module) _____ 77
Figure 11: Module Minimum 'Z' Height _____ 78
Figure 12: Carrier Board Connector PCB Footprint _____ 79
Figure 13: Heat Spreader Isometric View _____ 81
Figure 14: Heat Spreader Plan View _____ 82
Figure 15: Heat Sink Attachment Option _____ 83
Figure 16: Heat Spreader - 82mm x 80mm Module _____ 84
Figure 17: Power sequence diagram sleep and power button _____ 89
Figure 18: Power sequence diagram sleep, no power button _____ 89
Figure 19: Power sequence diagram power button _____ 90
Figure 20: Power sequence diagram, no power button _____ 91

1.5 List of Tables

Table 1: Revision History ____ 2
Table 2: Required and Optional Features ____ 16
Table 3: Signal Direction and Type Definitions ____ 17
Table 4: LVDS Signals ____ 20
Table 5: eDP Signals ____ 22
Table 6: MIPI-DSI Signals ____ 23
Table 7: LVDS / eDP / MIPI DSI Pin Sharing ____ 24
Table 8: Secondary HDMI Signals ____ 25
Table 9: DP++ Signals ____ 26
Table 10: Secondary HDMI / DP++ Pin Sharing ____ 27
Table 11: Third Display Interface DP++ Signals ____ 28
Table 12: MIPI-CSI Signals ____ 30
Table 13: MIPI-CSI Feature Connector Signals for 3rd Camera ____ 31
Table 14: MIPI-CSI Feature Connector Signals for 4th Camera ____ 32
Table 15: SDIO Signals ____ 34
Table 16: SPI0 Signals ____ 35
Table 17: SPI1 Signals ____ 35
Table 18: QSPI Signals ____ 36
Table 19: eSPI Signals ____ 38
Table 20: eSPI/SPI1/QSPI Pin Sharing ____ 38
Table 21: I2S0 Signals ____ 39
Table 22: I2S2 Signals ____ 40
Table 23: HDA Signals ____ 40
Table 24: I2S/HDA/SNDW Pin Sharing ____ 41
Table 25: I2C Signals ____ 42
Table 26: General Purpose I2C Signals ____ 42
Table 27: Serial Port Signals ____ 43
Table 28: CAN Bus Signals ____ 44
Table 29: USB Signal Assignments ____ 45
Table 30: USB configurations ____ 46
Table 31: USB Signals ____ 48
Table 32: PCI Express Signals ____ 51
Table 33: PCIe Link Configurations ____ 52
Table 34: PCIe Clock and Reset Assignments ____ 52
Table 35: SERDES Signals ____ 53
Table 36: PCIe Lane C&D / SERDES Pin Sharing ____ 54
Table 37: SATA Signals ____ 55
Table 38: Ethernet Signals GBE0 and GBE1 ____ 57
Table 39: Watchdog Signals ____ 58
Table 40: GPIO Signals ____ 59
Table 41: Alternative Use of GPIO Signals ____ 60
Table 42: GPIO Pin Sharing ____ 60
Table 43: Management Signals ____ 62
Table 44: Boot Select Signals ____ 63
Table 45: Control of Boot Sources ____ 64
Table 46: Power Signals ____ 65
Table 47: JTAG Signals ____ 66
Table 48: Module Pin-Out ____ 72
Table 49: Carrier Connectors ____ 73
Table 50: Heat Spreader Hole Reference ____ 82
Table 51: Power Rail Definitions ____ 87
Table 52: LVDS Color Mapping ____ 94

1.6 General Introduction

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor computer Module definition targeting applications that require low power, low costs, and high performance. The Modules will typically use ARM SOCs similar or the same as those used in many familiar devices such as tablet computers and smart phones. Alternative low power SOCs and CPUs, such as tablet oriented x86 devices and other RISC CPUs ***may*** be used as well. The Module power envelope is typically under 6W although designs up to about 15W are possible.

Two Module sizes are defined: 82mm x 50mm and 82mm x 80mm. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector (the connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, Gigabit Ethernet and dual channel LVDS display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

1.7 Purpose of This Document

This document defines the Module mechanical, electrical, signal and thermal parameters at a level of detail sufficient to provide a framework for SMARC Module and Carrier Board designs.

1.8 Document and Standards References

- ***CAN*** ("Controller Area Network") Bus Standards
  ISO 11898-1:2015 Road vehicles - Controller area network (CAN) - Part 1: Data link layer and physical signaling, (**www.iso.org**)
  ISO 11992-1:2019 Road vehicles - Interchange of digital information on electrical connections between towing and towed vehicles - Part 1: Physical and data-link layers (**www.iso.org**)
  SAE J2411: Feb 14, 2000, Single Wire CAN Network for Vehicle Applications (**www.sae.org**)
- ***MIPI CSI-2*** (Camera Serial Interface version 2) The MIPI CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***MIPI CSI-3*** (Camera Serial Interface version 3) The MIPI CSI-3 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***COM Express*** – the formal title for the COM Express specification is "PICMG® COM.0 COM Express Module Base Specification", Revision 3.0, March 31, 2017. This standard is owned and maintained by the PICMG ("PCI Industrial Computer Manufacturer's Group") (**www.picmg.org**)
- ***DisplayPort and Embedded DisplayPort*** These standards are owned and maintained by VESA ("Video Electronics Standards Association") (**www.vesa.org**)
- ***MIPI DSI*** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***eMMC*** ("Embedded Multi-Media Card") The eMMC electrical standard is defined by JEDEC JESD84-B51A and the mechanical standard by JESD84-C44 (**www.jedec.org**)
- ***eSPI*** ("Enhanced Serial Peripheral Interface") The eSPI Interface Base Specification is defined by Intel (**www.intel.com**)
- ***Fieldbus*** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: www.profibus.com/download/ and **www.can-cia.org**
- ***GBE MDI*** ("Gigabit Ethernet Medium Dependent Interface") This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (**www.ieee.org**)
- ***HDA (HD Audio)***, High Definition Audio Specification, Intel, Revision 1.0a, June 17, 2010 (**www.intel.com**)
- ***HDMI Specification***, Version 2.1, November 28, 2017 (**www.hdmi.org**)
- ***I2C Specification***, Version 6.0, April 4th 2014, Philips Semiconductor (now NXP) (**www.nxp.com**)
- ***I2S Bus Specification***, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (**www.nxp.com**)
- ***IEEE1588 - 2008***. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (***standards.ieee.org***)
- ***JTAG*** ("Joint Test Action Group") This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (**ieeexplore.ieee.org**)
- ***MXM3*** Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.1, NVidia Corporation
- ***PICMG® EEEP*** Embedded EEPROM Specification, Rev. 1.0, August 2010 (**www.picmg.org**)
- ***PCI Express*** Specifications (**www.pci-sig.org**)
- ***Serial ATA*** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (**www.sata-io.org**)

- ***SD Specifications*** Part 1 Physical Layer Simplified Specification, Version 6.00, Aug 29, 2018, SD Group and SD Card Association ("Secure Digital") (**www.sdcard.org**)
- ***SM Bus*** – "System Management Bus" Specification Version 3.1, March 19, 2018, System Management Interface Forum, Inc. (**www.smbus.org**)
- ***SPI Bus*** – "Serial Peripheral Interface" – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (**en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus**)
- ***USB*** Specifications (**www.usb.org**)

2 MODULE OVERVIEW

2.1 Form Factor Feature Summary

- Small form factor, low profile and low power edge-finger card format Module with pin-out optimized for ARM and x86 architecture processors; may also be used with low power, tablet oriented X86 and RISC devices.
- Two Module sizes:
  - 82mm x 50mm
  - 82mm x 80mm
- Carrier Board connector: 314 pin 0.5mm pitch R/A memory socket style connector
  - Originally defined for use with MXM3 graphics cards
  - SMARC Module pin-out is separate from and not related to MXM3 pin-out
  - Multiple sources for Carrier Board connector
  - Low cost
  - Low profile:
    - As low as 1.5mm (Carrier Board top to Module bottom)
    - Other stack height options available, including 2.7mm, 5mm, 8mm
    - Overall assembly height (Carrier Board top to tallest Module component) is less than 6mm
  - Excellent signal integrity – suitable for 2.5 GHz / 5 GHz / 8 GHz data rate signals such as PCIe Gen 1, Gen 2 and Gen 3.
  - Robust, vibration resistant connector
- Module input voltage range: 4.75V to 5.25V or 3.0V to 5.25V (module dependent)
  - Allows operation from 3.6V nominal Lithium-ion battery packs
  - Allows operation from 3.3V fixed DC supply
  - Allows operation from 5.0V fixed DC supply
  - Single supply (no separate standby voltage)
  - Module power pins allow 5A max
- Low power designs
  - Fanless
  - Passive cooling
  - Low standby power
  - Design for battery operation
  - 1.8V default I/O voltage

2.2 Module Interface Summary

The interfaces listed below are available per the Module pin definition. Some features are optional and availability is Module design dependent.

- Display Interfaces
  - Single or dual channel LVDS LCD 18 or 24 bit
    - Panel support signals (I2C, Power Enables, PWM)
    - Support for dual channel implementations
    - Multiplexing with eDP and MIPI DSI
  - HDMI port multiplexed with DP++ full featured implementation
  - Additional full featured DisplayPort++
- Camera Interfaces
  - Serial configuration: MIPI CSI (2 lane) + MIPI CSI (2 or 4 lane)
  - Two additional MIPI CSI interfaces available on optional connectors
- SDIO Interface
  - 4 bit SD card / SDIO interface with support lines
- SPI Interfaces
  - Two SPI interfaces
    - One maybe implemented as eSPI (x86) or QSPI (ARM)
- Audio Interfaces
  - First I2S interface
  - HDA interfaced multiplexed with second I2S or Soundwire interface
- I2C Interfaces
  - Seven I2C interfaces
    - Power Management
    - General Purpose
    - 4x Camera Interfaces (2x via SMARC connector and 2x via on module FFC connectors)
    - LCD Display ID
  - HDMI interface also has private I2C interface for HDMI use
- Asynchronous Serial Port Interfaces
  - Four asynchronous serial ports
    - Two supporting 2 wire handshake (RXD, TXD, RTS#, CTS#)
    - Two supporting data only (RXD, TXD)
    - Logic level interface

- CAN Bus Interfaces
  - Two CAN bus interfaces
    - Logic level signals from Module based CAN bus protocol controllers
    - RXD, TXD only
- USB Interfaces
  - Six ports total
  - Two sets of super speed signals for support of two USB 3.2 ports
  - Two ports supporting USB OTG (USB client or host)
  - USB support signals (VBUS enable / Over-current detects, OTG support signals)
- PCI Express
  - Four PCIe lanes
  - PCIe Gen1, Gen 2 or Gen 3 (Module dependent)
  - Three reference clock pairs
  - Three PCIe reset signals
  - Common PCIe wake signal (PCIE_WAKE#)
  - Two PCIE_CKREQ# signals for PCIE_A and PCIE_B
- SERDES
  - Alternative use of PCIE_C and PCIE_D as SERDES interface
  - One MDIO interface
- SATA Interface
  - One SATA interface
  - Gen 1, 2 or 3 (Module dependent)
- Gigabit Ethernet
  - Two analog GBE MDI interface
  - No magnetics on Module
  - LED support signals
  - CTREF (center tap reference voltage) for Carrier magnetics (if required by the Module GBE PHY)
  - Individual IEEE1588 trigger signal for each Ethernet interface to allow for enhanced real time applications. This utilizes a software definable pin (SDP) from the Ethernet controller.
- Wireless
  - Optional on module wireless functionality with designated area for antenna connections
- Watchdog Timer Interface
- General Purpose I/O
  - 14x GPIO signals

    - Specific alternate functions are assigned to some GPIOs
        - PWM / Tachometer capability
        - Camera support
        - HD Audio reset
- System and Power Management Signals
    - Reset out and Reset in
    - Power button in
    - Power source status
    - Module power state status
    - System management pins
    - Battery and battery charger management pins
    - Carrier Power On control
- Boot Source Select
    - Three pins to allow selection from Carrier Board
    - Select options to include boot from one of the following:
        - Module SPI
        - Module eMMC Flash
        - Module NAND / NOR Flash (vendor defined)
        - Module Remote Boot (Network or Serial Port, vendor defined)
        - Carrier SPI
        - Carrier SD Card
        - Carrier SATA
- JTAG functions for CPU debug and test are optionally implemented on separate small form factor connector

3 MODULE INTERFACE REQUIRED AND OPTIONAL FEATURES

3.1 Required and Optional Feature Table

Required and optional features for an SMARC Module are summarized in the table below.

"*Shall*"	indicates a mandatory requirement
"***Should***"	indicates a recommended but not mandatory requirement
"***May***"	indicates a lesser used optional interface
"***Alternate***"	indicates an optional interface, implemented on pins shared with another use

Feature	Sub Feature	Requirement	Notes
LVDS LCD	18 bit single channel	***Should***	Default Display (serial LVDS)
	24 bit single channel – 18 bit compatible	***Should***	
	24 bit single channel – standard color map	***May***	
	24 bit dual channel – 18 bit compatible	***May***	
	24 bit dual channel – standard color map	***May***	
DSI on LVDS Pins	DSI0 – 2 lane implementation	***May***	
	DSI0 – 4 lane implementation	***May***	
	DSI1 – 2 lane implementation	***May***	
	DSI1 – 4 lane implementation	***May***	
HDMI	HDMI display interface	***Should***	
DP on HDMI Pins		***May***	
DP++	DisplayPort++	***May***	
CSI	CSI0 – 2 lane	***May***	
	CSI1 – 2 lane implementation	***Should***	
	CSI1 – 4 lane implementation	***Should***	
	CSI2 – 2 lane implementation	***May***	
	CSI2 – 4 lane implementation	***May***	
	CSI3 – 2 lane implementation	***May***	
	CSI3 – 4 lane implementation	***May***	
SDIO	SDIO (4 bit, for SD cards)	***Should***	***May*** be Carrier boot device

SPI	SPI0	***Should***	***May*** be Carrier boot device
	SPI2	***Should***	
	QuadSPI	***Should***	
	eSPI	***Should***	***May*** be Carrier boot device
Audio	I2S0	***Should***	
	HDA or I2S2	***Should***	
I2C	Power Management	***Shall***	
	General Purpose	***Shall***	
	Camera 0/1/2/3	***Should***	
	LCD Display I/D	***Should***	
	HDMI	***Should***	Dedicated HDMI I2C interface
Serial Ports	SER0 (4 wire)	***Shall***	***May*** be used for optional serial console
	SER1 (2 wire)	***Shall***	***May*** be used for optional serial console
	SER2 (4 wire)	***Should***	
	SER3 (2 wire)	***Should***	
CAN Bus	CAN0	***May***	
	CAN1	***May***	
USB	USB0	***Shall***	
	USB1	***Should***	
	USB[2:5]	***May***	
PCIe	PCIE_A (x1 Gen 1 Root)	***Should***	
	PCIE_B (x1 Gen 1 Root)	***May***	
	PCIE_C (x1 Gen 1 Root)	***May***	
	PCIE_D (x1 Gen 1 Root)	***May***	
	PCIE_ Target operation	***May***	
	PCIE Gen 2 and Gen 3 operation	***May***	
SERDES	Alternative use of PCIE_C and/or PCIE_D	***May***	
SATA	SATA Gen 1	***Should***	***May*** be Carrier boot device
	SATA Gen 2 operation	***May***	
	SATA Gen 3 operation	***May***	
GBE	GBE0	***Should***	
	GBE1	***May***	

	IEEE 1588 Trigger Signals (GBE[0:1]_SDP)	***May***	
Watchdog	WDT Out	***Should***	
GPIO	GPIO[0:11]	***Shall***	
	GPIO[12:13]	***Should***	
	GPIO[0:11] interrupt capability	***Shall***	
	GPIO[12:13] interrupt capability	***Should***	
	GPIO Camera Support *(only when camera is supported)*	***Shall***	As appropriate for Module Camera implementation
	GPIO5 PWM capability	***Should***	
	GPIO6 Tachin capability	***Should***	
Management	System and power management features CARRIER_PWR_ON VIN_PWR_BAD#	***Shall***	See section 3.21'Management Pins' for details
	All other signals	***Should***	
Boot Select		***Shall***	
Force Recov		***Should***	See section 3.22 'Boot Select' for details
JTAG	JTAG connector on Module	***May***	Some vendors prefer test point access
RTC		***Should***	

Table 2: Required and Optional Features

3.2 Feature Fill Order

Features ***shall*** be filled in a low – to – high order, based on the signal group names. For example, there are four possible asynchronous serial ports, designated with signal prefixes SER0 to SER3. If a Module design implements only two SER ports, those would be SER0 and SER1. The PCIe links are designated PCIE_A, PCIE_B, PCIE_C and PCIE_D. If only one is implemented, it would be PCIE_A.

USB 3.2 port number 2 is the first in the fill order as the counting of USB 3.2 lines starts with number 2.

USB Super Speed operation is only defined for SMARC USB ports USB2 and USB3. Therefore, USB2 is the first in the fill order for USB Super Speed (aka USB 3.2) implementations on SMARC. If only two USB ports are implemented, USB1 can be skipped in the fill order to support one USB3.2 port on USB2.

Important exception, introduced with SMARC 2.1: The fill order for MIPI CSI is CSI1 (4 lane) first, then CSI0 (2 lane).

3.3 Signal Direction and Type Definitions

Term	Description
I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output
OD	Open drain
PU	PU (pull-up) resistor
PD	PD (pull-down) resistor
CMOS	Logic input or output
GBE MDI	Differential analog signaling for gigabit media dependent interface
DP	Low voltage differential signal for DisplayPort interface
D-PHY	Low voltage differential signal for MIPI CSI-2 cameras and DSI displays
M-PHY	Low voltage differential signal for MIPI CSI-3 cameras
LVDS	Low voltage differential signal for LCD displays
PCIE	Low voltage differential signal for PCIe
SATA	Low voltage differential signal for SATA
TMDS HDMI	Transition minimized differential signal for HDMI displays
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
VDD_IN	Main power source from Carrier to Module
3.3V	3.3V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
Sleep	Module is in its lowest power state
Runtime	Module is full on. CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
Standby	Module is in Standby State or higher

Table 3: Signal Direction and Type Definitions

3.4 Primary Display Interfaces

Pins used for LVDS LCD support ***may*** alternatively be used to support up to two Embedded DisplayPorts. The AC coupling required for eDP operation ***shall*** be done off-Module.

Pins used for LVDS LCD support ***may*** alternatively be used to support a MIPI DSI (Display Serial Interface). There is no AC coupling required for DSI operation.

3.4.1 LVDS

Single channel, dual channel or two single channel LVDS display panel interfaces are defined. The implementation of two single channel LVDS display interfaces is not expected to be common but is defined as an option for Module vendors. The LVDS interfaces support 18 and 24 bit display implementations.

In a Module implementation with two single LVDS channels, the panel EDID proms would be in conflict and measures need to be taken to avoid this. One possible solution is that the 2nd LVDS EDID prom could be read over the I2C_GP pin pair rather than the I2C_LCD pin pair.

The Module ***should*** implement an 18 / 24 bit LVDS output stream for the Primary display.

All 18 bit TFT panels use the same LVDS color mapping. Only 3 data pairs (LVDS[0:1]_[0:2] +/-) and the clock pair are needed to drive an 18 bit TFT panel.

Unfortunately, there are two 24 bit LVDS color mappings in the industry:

- Most significant color bits on the 4th LVDS data pair (LVDS[0:1]_[3] +/- here). This is the more common 24 bit mapping. It is not compatible with the 18 bit LVDS color mapping.
- Least significant color bits on the 4th LVDS data pair. This is compatible with the 18 LVDS color mapping.

Modules that implement LVDS ***shall*** implement single channel 18 bit LVDS; ***should*** implement a 24 bit "18 bit compatible" LVDS mapping and ***may*** implement the "MS bit on 4th LVDS pair" mapping. The second LVDS channel ***may*** be implemented.

Details on LVDS color mappings are provided in ***Section 8 Appendix A: LVDS LCD Color*** Mappings***.***

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LVDS0_0+ LVDS0_0- LVDS0_1+ LVDS0_1- LVDS0_2+ LVDS0_2- LVDS0_3+ LVDS0_3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary LVDS Channel Differential Pair Data Lines	O LVDS		Runtime		100 ohm differential termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.
LVDS0_CK+ LVDS0_CK-	S134 S135	Primary LVDS Channel Differential Pair Clock Lines	O LVDS		Runtime		100 ohm differential termination across the differential pair at the endpoint of the signal path, usually on the display assembly.
LCD0_VDD_EN	S133	Primary LVDS Channel Power Enable	O CMOS	1.8V	Runtime		Active high

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LCD0_BKLT_EN	S127	Primary LVDS Channel Backlight Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_PWM	S141	Primary LVDS Channel Brightness Control	O CMOS	1.8V	Runtime		Through Pulse Width Modulation (PWM)
LVDS1_0+ LVDS1_0- LVDS1_1+ LVDS1_1- LVDS1_2+ LVDS1_2- LVDS1_3+ LVDS1_3-	S111 S112 S114 S115 S117 S118 S120 S121	Secondary LVDS Channel Differential Pair Data Lines	O LVDS		Runtime		100 ohm differential termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.
LVDS1_CK+ LVDS1_CK-	S108 S109	Secondary LVDS Channel Differential Pair Clock Lines	O LVDS		Runtime		100 ohm differential termination across the differential pair at the endpoint of the signal path, usually on the display assembly.
LCD1_VDD_EN	S116	Secondary LVDS Channel Power Enable	O CMOS	1.8V	Runtime		Active high Only in use, when two separate LVDS ports are supported, please check Module user manual
LCD1_BKLT_EN	S107	Secondary LVDS Channel Backlight Enable	O CMOS	1.8V	Runtime		Active high Only in use, when two separate LVDS ports are supported, please check Module user manual
LCD1_BKLT_PWM	S122	Secondary LVDS Channel Brightness Control	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM) only in use, when two separate LVDS ports are supported, please check Module user manual
I2C_LCD_DAT	S140	DDC Data Line Used for Flat Panel Detection and Control	I/O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if two LVDS panels are used
I2C_LCD_CK	S139	DDC Clock Line Used for Flat Panel Detection and Control	I/O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if two LVDS panels are used

Table 4: LVDS Signals

3.4.2 eDP

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
eDP0_TX0+ eDP0_TX0- eDP0_TX1+ eDP0_TX1- eDP0_TX2+ eDP0_TX2- eDP0_TX3+ eDP0_TX3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary 4-Lane eDP Differential Pair Data Lines	O DP		Runtime		AC coupled off Module 100 nF DC blocking capacitors ***shall*** be placed on the Carrier.
eDP0_AUX+ eDP0_AUX-	S134 S135	Primary Bidirectional Channel used for Link Management and Device Control	I/O DP		Runtime		AC coupled off Module
LCD0_VDD_EN	S133	Primary Panel Power Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_EN	S127	Primary Panel Backlight Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_PWM	S141	Primary Panel Brightness Control	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)
eDP0_HPD	S144	Detection of Hot Plug / Unplug of Primary eDP Display and Notification of the Link Layer	I CMOS	1.8V	Runtime	PD 1M	Module must tolerate high level in stand-by mode
eDP1_TX0+ eDP1_TX0- eDP1_TX1+ eDP1_TX1- eDP1_TX2+ eDP1_TX2- eDP1_TX3+ eDP1_TX3-	S111 S112 S114 S115 S117 S118 S120 S121	Secondary 4-Lane eDP Differential Pair Data Lines	O DP		Runtime		AC coupled off Module 100 nF DC blocking capacitors ***shall*** be placed on the Carrier. Only in use, when two separate eDP ports are supported, please check Module user manual.
eDP1_AUX+ eDP1_AUX-	S108 S109	Secondary Bidirectional Channel used for Link Management and Device Control	I/O DP		Runtime		AC coupled off Module -only in use, when two separate eDP ports are supported, please check Module user manual.
LCD1_VDD_EN	S116	Secondary Panel Power Enable	O CMOS	1.8V	Runtime		Active high Only in use, when two separated eDP ports are supported. Please check Module user manual.
LCD1_BKLT_EN	S107	Secondary Panel Backlight Enable	O CMOS	1.8V	Runtime		Active high Only in use, when two separated eDP ports are supported. Please check Module user manual.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LCD1_BKLT_PWM	S122	Secondary Panel Brightness Control	O CMOS	1.8V	Runtime		Through Pulse Width Modulation (PWM) Only in use, when two separated eDP ports are supported. Please check Module user manual.
eDP1_HPD	S113	Detection of Hot Plug / Unplug of Secondary eDP Display and Notification of the Link Layer	I CMOS	1.8V	Runtime	PD 1M	Only in use, when two separated eDP ports are supported. Please check Module user guide! Module must tolerate high level in stand-by mode
I2C_LCD_DAT	S140	I2C Data to Read LCD Display EDID EEPROMs	I/O OD CMOS	1.8V	Runtime	PU 2k2	Possible EDID EEPROM Address conflicts may occur if multiple displays are implemented. Optional - eDP panel information is usually exchanged via the eDP auxiliary pair
I2C_LCD_CK	S139	I2C clock to read LCD display EDID EEPROMs	I/O OD CMOS	1.8V	Runtime	PU 2k2	Optional - eDP panel information is usually exchanged via the eDP auxiliary pair

Table 5: eDP Signals

3.4.3 MIPI DSI Display

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
DSI0_D0+ DSI0_D0- DSI0_D1+ DSI0_D1- DSI0_D2+ DSI0_D2- DSI0_D3+ DSI0_D3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary DSI Panel Differential Pair Data Lines	O D-PHY		Runtime		No blocking capacitors or termination required. Layout for 90 ohm differential impedance.
DSI0_CLK+ DSI0_CLK-	S134 S135	Primary DSI Panel Differential Pair Clock Lines	O D-PHY		Runtime		
LCD0_VDD_EN	S133	Primary Panel Power Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_EN	S127	Primary Panel Backlight Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_PWM	S141	Primary Panel Brightness Control	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)
DSI0_TE	S144	Primary DSI Panel Tearing Effect Signal	I CMOS	1.8V	Runtime	1M PD	
DSI1_D0+ DSI1_D0- DSI1_D1+ DSI1_D1- DSI1_D2+ DSI1_D2- DSI1_D3+ DSI1_D3-	S111 S112 S114 S115 S117 S118 S120 S121	Secondary DSI Panel Differential Pair Data Lines	O D-PHY		Runtime		No blocking capacitors or termination required. Layout for 90 ohm differential impedance.
DSI1_CLK+ DSI1_CLK-	S108 S109	Secondary DSI Panel Differential Pair Clock Lines	O D-PHY		Runtime		
LCD1_VDD_EN	S116	Secondary Panel Power Enable	O CMOS	1.8V	Runtime		Active high
LCD1_BKLT_EN	S107	Secondary Panel Backlight Enable	O CMOS	1.8V	Runtime		Active high
LCD1_BKLT_PWM	S122	Secondary Panel Brightness Control	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)
DSI1_TE	S113	Secondary DSI Panel Tearing Effect Signal	I CMOS	1.8V	Runtime	1M PD	
I2C_LCD_DAT	S140	DDC Data Line Used for Flat Panel Detection and Control	I/O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if two LVDS panels are used
I2C_LCD_CK	S139	DDC Clock Line Used for Flat Panel Detection and Control	I/O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if two LVDS panels are used

Table 6: MIPI-DSI Signals

3.4.4 LVDS / eDP / MIPI DSI Pin Sharing

Pin #	LVDS Signal Name	MIPI DSI Signal Name	eDP Signal Name
S125	LVDS0_0+	DSI0_D0+	eDP0_TX0+
S126	LVDS0_0-	DSI0_D0-	eDP0_TX0-
S128	LVDS0_1+	DSI0_D1+	eDP0_TX1+
S129	LVDS0_1 -	DSI0_D1-	eDP0_TX1-
S131	LVDS0_2+	DSI0_D2+	eDP0_TX2+
S132	LVDS0_2-	DSI0_D2-	eDP0_TX2-
S137	LVDS0_3+	DSI0_D3+	eDP0_TX3+
S138	LVDS0_3-	DSI0_D3-	eDP0_TX3-
S134	LVDS0_CK+	DSI0_CLK+	eDP0_AUX+
S135	LVDS0_CK-	DSI0_CLK-	eDP0_AUX-
S133	LCD0_VDD_EN	LCD0_VDD_EN	LCD0_VDD_EN
S127	LCD0_BKLT_EN	LCD0_BKLT_EN	LCD0_BKLT_EN
S141	LCD0_BKLT_PWM	LCD0_BKLT_PWM	LCD0_BKLT_PWM
S144	-	DSI0_TE	eDP0_HPD
S111	LVDS1_0+	DSI1_D0+	eDP1_TX0+
S112	LVDS1_0-	DSI1_D0-	eDP1_TX0-
S114	LVDS1_1+	DSI1_D1+	eDP1_TX1+
S115	LVDS1_1 -	DSI1_D1-	eDP1_TX1-
S117	LVDS1_2+	DSI1_D2+	eDP1_TX2+
S118	LVDS1_2-	DSI1_D2-	eDP1_TX2-
S120	LVDS1_3+	DSI1_D3+	eDP1_TX3+
S121	LVDS1_3-	DSI1_D3-	eDP1_TX3-
S108	LVDS1_CK+	DSI1_CLK+	eDP1_AUX+
S109	LVDS1_CK-	DSI1_CLK-	eDP1_AUX-
S116	LCD1_VDD_EN	LCD1_VDD_EN	LCD1_VDD_EN
S107	LCD1_BKLT_EN	LCD1_BKLT_EN	LCD1_BKLT_EN
S122	LCD1_BKLT_PWM	LCD1_BKLT_PWM	LCD1_BKLT_PWM
S113	-	DSI1_TE	eDP1_HPD
S140	I2C_LCD_DAT	I2C_LCD_DAT	I2C_LCD_DAT
S139	I2C_LCD_CK	I2C_LCD_CK	I2C_LCD_CK

Table 7: LVDS / eDP / MIPI DSI Pin Sharing

3.5 Secondary Display Interface

The SMARC HDMI pins ***may*** alternatively be used for DisplayPort++ (DP++) operation. This is Module vendor dependent.

3.5.1 HDMI

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
HDMI_D2+ HDMI_D2- HDMI_D1+ HDMI_D1- HDMI_D0+ HDMI_D0-	P92 P93 P95 P96 P98 P99	HDMI Port, Differential Pair Data Lines	O TMDS HDMI		Runtime		
HDMI_CK+ HDMI_CK-	P101 P102	HDMI Port, Differential Pair Clock Lines	O TMDS HDMI		Runtime		
HDMI_CTRL_CK	P105	I2C_CLK Line Dedicated to HDMI	I/O OD CMOS	1.8V	Runtime	PU 100K	Level shifter FET and 5V PU resistor ***shall*** be placed between the Module and the HDMI connector. Stronger pull-up is demanded to the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete Carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_CTRL_DAT	P106	I2C_DAT Line Dedicated to HDMI	I/O OD CMOS	1.8V	Runtime	PU 100K	Level shifter FET and 5V PU resistor ***shall*** be placed between the Module and the HDMI connector. Stronger pull-up is demanded to the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete Carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_HPD	P104	HDMI Hot Plug Active High Detection Signal that Serves as an Interrupt Request	I CMOS	1.8V	Runtime	PD 1M	Important: Module ***shall*** tolerate high level in stand-by mode

Table 8: Secondary HDMI Signals

HDMI displays uses 5V I2C signaling. The Module HDMI_CTRL_DAT and HDMI_CTRL_CK signals need to be level translated on the Carrier from the Module 1.8V level. A similar consideration applies to the HDMI_HPD signal. There are a number of single chip devices on the market that perform ESD protection and control signal level shifting for HDMI interfaces. The Texas Instruments TPD12S016 is one such device.

3.5.2 DP++

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
DP1_LANE0+ DP1_LANE0- DP1_LANE1+ DP1_LANE1- DP1_LANE2+ DP1_LANE2- DP1_LANE3+ DP1_LANE3-	P92 P93 P95 P96 P98 P99 P101 P102	Secondary DP Port Differential Pair Data Lines	O DP		Runtime		AC coupled off Module 100 nF DC blocking capacitors ***shall*** be placed on the Carrier
DP1_AUX+	P105	Secondary DP Port Bidirectional Channel used for Link Management and Device Control	I/O DP	3.3V	Runtime	PD 100k	AC coupled on Module If DP1_AUX_SEL=0 (DP mode): AC coupled on module, 100k PD. If DP1_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board.
DP1_AUX-	P106	Secondary DP Port Bidirectional Channel used for Link Management and Device Control	I/O DP	3.3V	Runtime	PU 100k	AC coupled on Module If DP1_AUX_SEL=0 (DP mode): AC coupled on module, 100k PU. If DP1_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board.
DP1_HPD	P104	DP Hot Plug Detect Input	I CMOS	1.8V	Runtime	PD 1M	Module must tolerate high level in stand-by mode. The Carrier ***shall*** include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP1_AUX_SEL	P107	Strapping Signal to Enable Either HDMI or DP Output	I CMOS	1.8V	Runtime	PD 1M	Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations. Driven to 1.8V on Carrier for HDMI mode. Module must tolerate high level in stand-by mode. ***Should*** be connected to pin 13 of the DisplayPort connector to enable a dual-mode DisplayPort interface.

Table 9: DP++ Signals

Dual Mode (HDMI and DisplayPort on the same pins) implementations ***may*** be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

3.5.3 Secondary HDMI / DP++ Pin Sharing

Pin #	HDMI Signal Name	DP++ Name
P92	HDMI_D2+	DP1_LANE0+
P93	HDMI_D2-	DP1_LANE0-
P95	HDMI_D1+	DP1_LANE1+
P96	HDMI_D1-	DP1_LANE1-
P98	HDMI_D0+	DP1_LANE2+
P99	HDMI_D0-	DP1_LANE2-
P101	HDMI_CK+	DP1_LANE3+
P102	HDMI_CK-	DP1_LANE3-
P105	HDMI_CTRL_CK	DP1_AUX+
P106	HDMI_CTRL_DAT	DP1_AUX-
P104	HDMI_HPD	DP1_HPD

Table 10: Secondary HDMI / DP++ Pin Sharing

3.6 Third Display Interface

3.6.1 DP++

A DP++ interface can output signals that are formatted per either DP or HDMI / DVI protocols. The signal levels are DP compliant. For DP use, off-Module coupling caps are needed on the 4 DP display data lanes. A Carrier Board level translator is usually needed for HDMI / DVI operation.

DP++ or DisplayPort++ (also named as Dual-mode DisplayPort) can directly output HDMI and DVI signals. The level adaptation can be implemented on the Carrier or via plug in cable adapter. In case of Carrier Board implementation, a level shifter adjusts the I/O voltage to HDMI/DVI compliant signal levels. A dual-mode chipset switches to DVI/HDMI mode (4-lane main DisplayPort link and AUX channel) if a DVI or HDMI passive adapter is detected (by DP0_AUX_SEL).

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
DP0_LANE0+ DP0_LANE0- DP0_LANE1+ DP0_LANE1- DP0_LANE2+ DP0_LANE2- DP0_LANE3+ DP0_LANE3-	S93 S94 S96 S97 S99 S100 S102 S103	Primary DP Port Differential Pair Data Lines	O DP		Runtime		AC coupled off Module 100 nF DC blocking capacitors ***shall*** be placed on the Carrier
DP0_AUX+	S105	Primary DP Port Bidirectional Channel used for Link Management and Device Control	I/O DP	3.3V	Runtime	PD 100k	AC coupled on Module If DP0_AUX_SEL=0 (DP mode): AC coupled on module, 100k PD. If DP0_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board.
DP0_AUX-	S106	Primary DP Port Bidirectional Channel used for Link Management and Device Control	I/O DP	3.3V	Runtime	PU 100k	AC coupled on Module If DP0_AUX_SEL=0 (DP mode): AC coupled on module, 100k PU. If DP0_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board.
DP0_AUX_SEL	S95	Auxiliary Selection	I CMOS	1.8V	Runtime	PD 1M	Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations Module must tolerate high level in stand-by mode. ***Should*** be connected to pin 13 of the DisplayPort connector to enable a dual-mode DisplayPort interface.
DP0_HPD	S98	DP Hot Plug Detect Input	I CMOS	1.8V	Runtime	PD 1M	Module must tolerate high level in stand-by mode. The Carrier ***shall*** include a blocking FET on DP[0:1]_HPD to prevent back-drive current from damaging the Module.

Table 11: Third Display Interface DP++ Signals

3.7 Camera Interfaces

SMARC 2.0 defines four MIPI CSI serial camera interfaces. The defined CSI0 interface supports up to two differential data lanes (CSI0_D[0:1]+/- signals). CSI1 ***may*** be implemented with up to four differential data lanes (CSI1_D[0:3]+/- signals) to support higher resolution cameras.

Both MIPI CSI interfaces support MIPI-CSI 2.0 but are also prepared to support the implementation of MIPI-CSI 3.0. Both standards continue to evolve (see **http://mipi.org/specifications/camera-interface**). While MIPI-CSI 2.0 utilizes an I2C bus (I2C_CAM[0:1]) to communicate with the camera the MIPI-CSI 3.0 uses a differential data lane (CSI[0:1]_TX+/-).

3.7.1 1st and 2nd MIPI CSI on SMARC Edge Connector

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI0_RX0+ CSI0_RX0- CSI0_RX1+ CSI0_RX1-	S11 S12 S14 S15	CSI0 differential input	I D-PHY / I M-PHY		Runtime		
CSI0_CK+ CSI0_CK-	S8 S9	CSI0 differential clock input (point to point)	I D-PHY		Runtime		
I2C_CAM0_DAT / CSI0_TX-	S7	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required
I2C_CAM0_CK / CSI0_TX+	S5	I2C clock for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required
CAM0_PWR#	P108	Camera 0 Power Enable, active low output.	O CMOS	1.8V	Runtime		Shared with GPIO0
CAM0_RST#	P110	Camera 0 reset, active low output	O CMOS	1.8V	Runtime		Shared with GPIO2
CSI1_RX0+ CSI1_RX0- CSI1_RX1+ CSI1_RX1- CSI1_RX2+ CSI1_RX2- CSI1_RX3+ CSI1_RX3-	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input (point to point)	I D-PHY / I M-PHY		Runtime		

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock input (point to point)	I D-PHY		Runtime		
I2C_CAM1_DAT / CSI1_TX-	S2	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_DAT which requires PU MIPI-CSI 3.0 mode uses CSI1_TX-, no PU required
I2C_CAM1_CK / CSI1_TX+	S1	I2C clock for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_CK which requires PU MIPI-CSI 3.0 mode uses CSI1_TX+, no PU required
CAM1_PWR#	P109	Camera 1 Power Enable, active low output.	O CMOS	1.8V	Runtime		Shared with GPIO1
CAM1_RST#	P111	Camera 1 reset, active low output	O CMOS	1.8V	Runtime		Shared with GPIO3
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		

Table 12: MIPI-CSI Signals

MIPI CSI Configuration CSI-2 and CSI-3

The newer version of the MIPI Camera Serial Interface CSI-3 no longer uses an I2C bus to transmit commands and configurations to the camera. A newly defined high-speed differential signal pair is used instead.

Serial Cameras In

Two MIPI CSI camera interfaces are supported. The CSI0 interface supports two lanes, the CSI1 interface supports 4 lanes. MIPI CSI 2.0 and MIPI CSI 3.0 are supported. With SMARC 2.1 the fill order changed to CSI1 first.

3.7.2 3rd and 4th MIPI CSI on optional feature connector

Two identical feature connectors ***may*** be used to connect two extra MIPI cameras by flat foil cables

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI2_RX0+ CSI2_RX0- CSI2_RX1+ CSI2_RX1- CSI2_RX2+ CSI2_RX2- CSI2_RX3+ CSI2_RX3-	4 5 7 8 10 11 13 14	CSI2 differential input (point to point)	I D-PHY / I M-PHY		Runtime		
CSI2_CK+ CSI2_CK-	16 17	CSI2 differential clock input (point to point)	I D-PHY		Runtime		
I2C_CAM2_DAT / CSI2_TX-	20	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C which requires PU MIPI-CSI 3.0 mode uses a differential pair, no PU required
I2C_CAM2_CK / CSI2_TX+	19	I2C clock for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C which requires PU MIPI-CSI 3.0 mode uses a differential pair, no PU required
CAM2_PWR#	21	Camera 2 Power Enable, active low output.	O CMOS	1.8V	Runtime		
CAM2_RST#	12	Camera 2 reset, active low output	O CMOS	1.8V	Runtime		
CAM2_MCK	22	Master clock output	O CMOS	1.8V	Runtime		
CAM2_VCC	1, 2	Power		3.3V	Runtime		VCC Power for MIPI Camera Minimum current: 100mA [1]
GND	3, 6, 9, 15, 18	Ground					GND for MIPI Camera power and signals

Table 13: MIPI-CSI Feature Connector Signals for 3rd Camera

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI3_RX0+ CSI3_RX0- CSI3_RX1+ CSI3_RX1- CSI3_RX2+ CSI3_RX2- CSI3_RX3+ CSI3_RX3-	4 5 7 8 10 11 13 14	CSI3 differential input (point to point)	I D-PHY / I M-PHY		Runtime		
CSI3_CK+ CSI3_CK-	16 17	CSI3 differential clock input (point to point)	I D-PHY		Runtime		
I2C_CAM3_DAT / CSI3_TX-	20	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C which requires PU MIPI-CSI 3.0 mode uses a differential pair, no PU required
I2C_CAM3_CK / CSI3_TX+	19	I2C clock for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C which requires PU MIPI-CSI 3.0 mode uses a differential pair, no PU required
CAM3_PWR#	21	Camera 3 Power Enable, active low output.	O CMOS	1.8V	Runtime		
CAM3_RST#	12	Camera 3 reset, active low output	O CMOS	1.8V	Runtime		
CAM3_MCK	22	Master clock output	O CMOS	1.8V	Runtime		
CAM3_VCC	1, 2	Power		3.3V	Runtime		VCC Power for MIPI Camera Minimum current: 100mA [1]
GND	3, 6, 9, 15, 18	Ground					GND for MIPI Camera power and signals

Table 14: MIPI-CSI Feature Connector Signals for 4th Camera

[1] Electrical Specification of 3.3V Supply

The Host System (SMARC™ module) shall provide 3.3V +/-5% over a maximum load current of 100mA. If a connected camera system will draw more power, it should either be supplied with an individual power-supply or the vendor should be asked for the maximum current capability.

Note:

The FFC cable used can limit the available current for the cameras. Please check the manufacturer maximum ratings for the used cables.

3.7.2.1 MIPI CSI feature connector

A 22 pin FPC connector with 22 pins ***may*** be used as feature connector for extra MIPI CSI signals.
TE part number: 2-1734592-2 or compatible (i.e. FDS0520 from company Sunfun or MWAFC07-S22FXA-HF from company 勝 達 電 子).

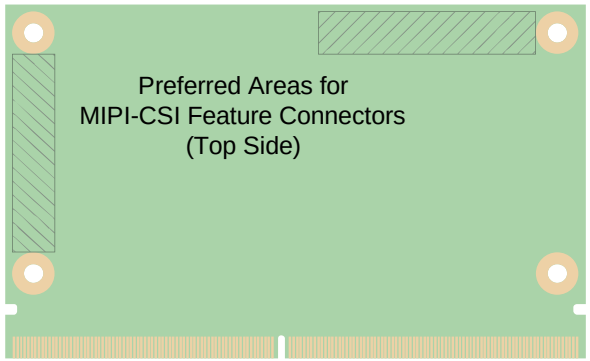


Figure 1: MIPI CSI feature connector placement (82x50mm Module)

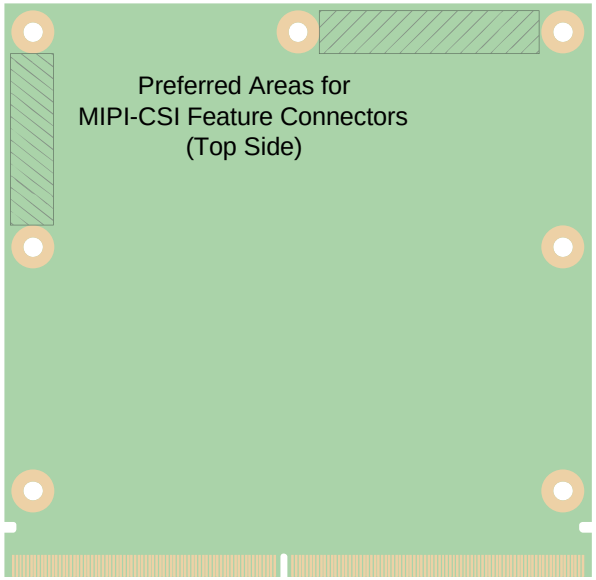


Figure 2: MIPI CSI feature connector placement (82x80mm Module)

3.8 SDIO Card (4 bit) Interface

The SD Card / SDIO interface can support SD Cards as storage devices or additionally SDIO functionality. A SDIO (Secure Digital Input Output) card is an extension of the SD specification to cover I/O functions. SDIO cards are only fully functional in host devices designed to support their input-output functions. These devices can use the SD slot to support GPS receivers, modems, barcode readers, radio tuners, RFID readers, digital cameras, and interfaces to Wi-Fi, Bluetooth, Ethernet, and IrDA.

The SDIO and SD interfaces are mechanically and electrically identical. Host devices built for SDIO cards generally accept SD memory cards without I/O functions. However, the reverse is not true, because host devices need suitable drivers and applications to support the card's I/O functions.

The Carrier SDIO Card ***may*** be selected as the Boot Device – see Table 45 'Control of Boot Sources' on page 64.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	P39 P40 P41 P42	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller ***may*** detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_WP	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	1.8V or 3.3V	Runtime	PU 10k	
SDIO_CMD	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller ***may*** detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_CD#	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	1.8V or 3.3V	Runtime	PU 10k	
SDIO_CK	P36	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_PWR_EN	P37	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	3.3V	Runtime		***Should*** be driven low in Standby Mode by the Module

Table 15: SDIO Signals

Note:

There are SD Cards with a 1.8V I/O voltage (UHS-I). SDIO controllers supporting these cards will adjust the I/O voltage levels.

3.9 SPI Interfaces

3.9.1 SPI0

The Carrier SPI0 device ***may*** be selected as the Boot Device – see Table 45 'Control of Boot Sources' on page 64

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI0_CS0#	P43	SPI0 Master Chip Select 0	O CMOS	1.8V	Standby		This signal can be used to select Carrier SPI as boot device. (***Shall***)
SPI0_CS1#	P31	SPI0 Master Chip Select 1	O CMOS	1.8V	Standby		(***Should***)
SPI0_CK	P44	SPI0 Clock	O CMOS	1.8V	Standby		
SPI0_DIN	P45	SPI0 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
SPI0_DO	P46	SPI0 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

Table 16: SPI0 Signals

3.9.2 SPI1

SPI1 is the general-purpose SPI bus.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI1_CS0#	P54	SPI1 Master Chip Select 0	O CMOS	1.8V	Standby		(***Shall***)
SPI1_CS1#	P55	SPI1 Master Chip Select 1	O CMOS	1.8V	Standby		(***Should***)
SPI1_CK	P56	SPI1 Clock	O CMOS	1.8V	Standby		
SPI1_DIN	P57	SPI1 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
SPI1_DO	P58	SPI1 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

Table 17: SPI1 Signals

3.9.3 QSPI

The QSPI is a controller extension for the SPI Bus. The difference is that it uses a data queue with programmable queue pointers that allow the data transfers without the CPU intervention. It also has a wrap-around mode that allows continuous transfers and from the queue with no CPU intervention. The peripherals appear to the CPU as memory-mapped parallel devices. This is useful in application such as controlling an analog to digital converter. QSPI has some more programmable features like chip select and transfer length delay. – see Table 20: eSPI/SPI1/QSPI Pin SharingControl of Boot Sources' for further information regarding the different operation modes of the SPI interface.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
QSPI_CS0#	P54	QSPI Master Chip Select 0	O CMOS	1.8V	Standby		(***Shall***)
QSPI_CS1#	P55	QSPI Master Chip Select 1	O CMOS	1.8V	Standby		(***Should***)
QSPI_CK	P56	QSPI Clock	O CMOS	1.8V	Standby		
QSPI_IO_3	S57	QSPI Data input / output	I/O CMOS	1.8V	Standby		
QSPI_IO_2	S56	QSPI Data input / output	I/O CMOS	1.8V	Standby		
QSPI_IO_1	P57	QSPI Data input / output	I/O CMOS	1.8V	Standby		
QSPI_IO_0	P58	QSPI Data input / output	I/O CMOS	1.8V	Standby		

Table 18: QSPI Signals

3.9.4 eSPI

eSPI stands for Enhanced Serial Peripheral Interface. It was introduced to replace the legacy LPC Bus.

It is defined to meet the following requirements:

- Low Power: The interface may be active in all S0-S5 system states. The power consumed when the bus is operating in S3-S5 system states must be very low to meet the power requirements of these low power system states. When the interface is not transmitting or receiving, it should consume a negligible amount of power (at system level).
- Pin Count Reduction: Moving LPC devices over to the eSPI interface facilitates the removal of LPC pins in the longer term. On top of that messaging through sideband pins needed for communication between the chipset and slave devices (such as EC, BMC and SIO) is converted to in-band messages, resulting in further pin count reduction.
- Medium Bandwidth: The bus bandwidth needs to be higher than that of the Low Pin Count (LPC) bus.
- LPC Replacement: Supports all the capabilities needed to replace the parallel LPC interface. However, 8237 DMA and Firmware Hub (FWH) are not supported over this interface.
- Sideband Pins as In-Band Messaging: Facilitates the removal of sideband pins for communication between chipset and slave devices by converting this communication into in-band messages sent over the eSPI bus.
- Real-Time Flash Sharing: Supports flash sharing based on partition-able memory mapping. Allows real-time operational access by chipset and slave devices.
- Chipset and Slave Devices SMBus Replacement: Supports tunneling of all SMBus communication between chipset and slave devices over the new interface as in-band messages.
- Scalable bandwidth: Allows the bandwidth to be scaled based on application needs to optimize power versus performance. This could be done through frequency scaling or varying the number of active data pins.
- Low Voltage I/O Buffer: eSPI uses the same I/O buffer as Serial Peripheral Interface (SPI). The I/O buffer will support only 1.8V mode of operation for the eSPI bus.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
ESPI_CS0#	P54	ESPI1 Master Chip Select 0	O CMOS	1.8V	Standby		(***Shall***)
ESPI_CS1#	P55	ESPI1 Master Chip Select 1	O CMOS	1.8V	Standby		(***Should***)
ESPI_CK	P56	ESPI Master Clock Output	O CMOS	1.8V	Standby		Pin provides reference timing for all serial input / output operations.
ESPI_RESET#	S58	ESPI Reset	O CMOS	1.8V	Standby		Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves
ESPI_ALERT0# ESPI_ALERT1#	S43 S44	ESPI ALERT	I OD CMOS	1.8V	Standby	4.7k PU	These pins are used by eSPI slaves to request service from eSPI master. Open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.
ESPI_IO_0 ESPI_IO_1 ESPI_IO_2 ESPI_IO_3	P58 P57 S56 S57	ESPI Master Data Input / Output	I/O CMOS	1.8V	Standby		In Single I/O mode, ESPI_IO_0 is the eSPI master output / eSPI slave input (MOSI) whereas ESPI_IO_1 is the SPI master input / eSPI slave output (MISO).

Table 19: eSPI Signals

3.9.5 eSPI/SPI1/QSPI Pin Sharing

Pin #	eSPI Signal Name	SPI1 Name	QSPI Name
P58 P57 S56 S57	ESPI_IO_0 ESPI_IO_1 ESPI_IO_2 ESPI_IO_3	SPI1_DO SPI1_DIN - -	QSPI_IO_0 QSPI_IO_1 QSPI_IO_2 QSPI_IO_3
S43 S44	ESPI_ALERT0# ESPI_ALERT1#	- -	- -
S58	ESPI_RESET	-	-
P56	ESPI_CK	SPI1_CK	QSPI_CK
P55	ESPI_CS1#	SPI1_CS1#	QSPI_CS1#
P54	ESPI_CS0#	SPI1_CS0#	QSPI_CS0#

Table 20: eSPI/SPI1/QSPI Pin Sharing

Note: Please refer to the **SMARC Design Guide** 2.1.1 (Chapter 11.6) for further information regarding the implementation of SPI and the recommended bus topology considerations.

3.10 Audio

Two audio interfaces are defined. One I2S interface is pin shared with HDA. I2S1 from SMARC V1.1 has been deprecated.

The I2S interface is typically used for ARM processor implementation. HDA is typically used for x86 processor implementations. The HDA interface ***may*** also be used for a second I2S interface.

3.10.1 I2S0

Two I2S interfaces are defined. These are typically used for digital audio I/O and other modest bandwidth functions. A common audio master clock signal is also defined.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2S0_LRCK	S39	I2S0 Left & Right Synchronization Clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
I2S0_SDOUT	S40	I2S0 Digital Audio Output	O CMOS	1.8V	Runtime		
I2S0_SDIN	S41	I2S0 Digital Audio Input	I CMOS	1.8V	Runtime		
I2S0_CK	S42	I2S0 Digital Audio Clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AUDIO_MCK	S38	Master Clock Output to I2S Codec(s)	O CMOS	1.8V	Runtime		

Table 21: I2S0 Signals

3.10.2 I2S2

The second I2S interface can also be implemented as HDA or Soundwire interface.
The master clock output (AUDIO_MCK) is shared between both I2S interfaces.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2S2_LRCK	S50	I2S2 Left & Right Synchronization Clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
I2S2_SDOUT	S51	I2S2 Digital Audio Output	O CMOS	1.8V	Runtime		
I2S2_SDIN	S52	I2S2 Digital Audio Input	I CMOS	1.8V	Runtime		
I2S2_CK	S53	I2S2 Digital Audio Clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
AUDIO_MCK	S38	Master Clock Output to I2S Codec(s)	O CMOS	1.8V	Runtime		

Table 22: I2S2 Signals

3.10.3 HDA

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
HDA_SYNC	S50	High Definition Audio Sample synchronization clock to codec	I/O CMOS	1.8V / 1.5V	Runtime		SMARC requires 1.5V or 1.8V HD Audio signaling. Please check with your Module vendor if 1.5V or 1.8V are supported and use an audio codec that is capable to support the regarding I/O voltage. The SMARC HD Audio pins are shared with the I2S2 pins, which are defined to be 1.8V. This specification ignores the discrepancy between the 1.5V and 1.8V signaling, as the chance of damage in mismatched systems is negligible.
HDA_SDO	S51	High Definition Audio data out to codec	O CMOS	1.8V / 1.5V	Runtime		
HDA_SDI	S52	High Definition Audio data in from codec"	I/O CMOS	1.8V / 1.5V	Runtime		
HDA_CK	S53	High Definition Audio clock to codec	O CMOS	1.8V / 1.5V	Runtime		
HDA_RST#	P112	High Definition Audio Reset Output to Codec, low active.	O CMOS	1.8V / 1.5V	Runtime		

Table 23: HDA Signals

3.10.4 Soundwire

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SNDW_CLK1	S50	Clock for Soundwire 1 transactions	O CMOS	1.8V	Runtime		
SNDW_DAT1	S51	Soundwire 1 bi-directional PCM audio data lane	I/O CMOS	1.8V	Runtime		
SNDW_DAT0	S52	Soundwire 0 bi-directional PCM audio data lane	I/O CMOS	1.8V	Runtime		
SNDW_CLK0	S53	Clock for Soundwire 0 transactions	O CMOS	1.8V	Runtime		

3.10.5 I2S/HDA/SNDW Pin Sharing

Pin #	I2S2 Signal Name	HDA Signal Name	Soundwire Signal Name
S50	I2S2_LRCK	HDA_SYNC	SNDW_CLK1
S51	I2S2_SDOUT	HDA_SDO	SNDW_DAT1
S52	I2S2_SDIN	HDA_SDI	SNDW_DAT0
S53	I2S2_CK	HDA_CK	SNDW_CLK0
P112	-	HDA_RST#	-

Table 24: I2S/HDA/SNDW Pin Sharing

Note: The numbering of the secondary, alternative I2S interface is #2 because the I2S interface #1 from SMARC 1.1 was removed for SMARC 2.0.

Per the HD Audio specification, HD Audio ***may*** be run at either 1.5V or 3.3V. SMARC requires 1.5V or 1.8V HD Audio signaling. Please check with your Module vendor if 1.5V or 1.8V are supported and use an audio codec that is capable to support the regarding I/O voltage. The SMARC HD Audio pins are shared with the I2S2 and Soundwire[0:1] pins, which are defined to be 1.8V. This specification ignores the discrepancy between the 1.5V and 1.8V signaling, as the chance of damage in mismatched systems is negligible.

ARM SOCs generally run I2S audio and will likely use 1.8V signaling. X86 SOCs generally run 1.5V signal levels on the HD Audio interface.

3.11 I2C Interfaces

The Module supports upto eight I2C interfaces, per the following table. Except for the LCD and HDMI Module I2C interfaces, the I2C ports ***should*** be multi-master capable. Data rates of 100 kHz and 400 kHz ***should*** be supported.

I2C Port	Primary Purpose	Alternate Use	Note
I2C_PM	Power Management Support	System configuration management	see section 3.21 ‘Management Pins’ on page 61
I2C_CAM0 I2C_CAM1 I2C_CAM2 I2C_CAM3	Camera Support	General Purpose	see section 3.7.1 ‘1st and 2nd MIPI CSI’ on page 29
I2C_GP	General Purpose Use		
I2C_LCD	LCD Display Support	General Purpose	see section 3.4.1 ‘LVDS’ on page 19
HDMI_CTRL	HDMI Control		see section 3.5.1 ‘HDMI’ on page 25

Table 25: I2C Signals

All I2C interfaces but the I2C_GP interface are described in the section served by that I2C link (LCD, HDMI, Camera Interface, etc.). The I2C_GP Module interface consists of the following two pins:

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2C_GP_DAT	S49	General Purpose I2C Data Signal	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_GP_CK	S48	General Purpose I2C Clock Signal	I/O OD CMOS	1.8V	Runtime	PU 2k2	

Table 26: General Purpose I2C Signals

3.12 Asynchronous Serial Ports

Module pins for up to four asynchronous serial ports are defined. The ports are designated SER0 – SER3. Ports SER0 and SER2 are 4 wire ports (2 data lines and 2 handshake lines). Ports SER1 and SER3 are 2 wire ports (data only).

If a serial console of the bootloader/BIOS is to be implemented for the module the SER0 or SER1 ports ***may*** be used for this function.
For further information regarding the implemented serial console port please contact the module vendor.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SER0_TX	P129	Asynchronous Serial Data Output Port 0	O CMOS	1.8V	Runtime		
SER0_RX	P130	Asynchronous Serial Data Input Port 0	I CMOS	1.8V	Runtime	PU 100k	
SER0_RTS#	P131	Request to Send Handshake Line for Port 0	O CMOS	1.8V	Runtime		
SER0_CTS#	P132	Clear to Send Handshake Line for Port 0	I CMOS	1.8V	Runtime	PU 100k	
SER1_TX	P134	Asynchronous Serial Data Output Port 1	O CMOS	1.8V	Runtime		
SER1_RX	P135	Asynchronous Serial Data Input Port 1	I CMOS	1.8V	Runtime	PU 100k	
SER2_TX	P136	Asynchronous Serial Data Output Port 2	O CMOS	1.8V	Runtime		
SER2_RX	P137	Asynchronous Serial Data Input Port 2	I CMOS	1.8V	Runtime	PU 100k	
SER2_RTS#	P138	Request to Send Handshake Line for Port 2	O CMOS	1.8V	Runtime		
SER2_CTS#	P139	Clear to Send Handshake Line for Port 2	I CMOS	1.8V	Runtime	PU 100k	
SER3_TX	P140	Asynchronous Serial Data Output Port 3	O CMOS	1.8V	Runtime		
SER3_RX	P141	Asynchronous Serial Data Input Port 3	I CMOS	1.8V	Runtime	PU 100k	

Table 27: Serial Port Signals

3.13 CAN Bus

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAN0_TX	P143	CAN Port 0 Transmit Output	O CMOS	1.8V	Runtime		
CAN0_RX	P144	CAN Port 0 Receive Input	I CMOS	1.8V	Runtime		
CAN1_TX	P145	CAN Port 1 Transmit Output	O CMOS	1.8V	Runtime		
CAN1_RX	P146	CAN Port1 Receive Input	I CMOS	1.8V	Runtime		

Table 28: CAN Bus Signals

3.14 USB Interfaces

SMARC 2.0 provides six sets of USB 2.0 signals and two sets of USB 3.2 Super Speed signals. USB OTG and USB Client functionalities are also supported.

USB 3.2 is supported for the USB ports 2 and 3. For implementation of an USB 3.2 OTG or USB 3.2 host interface the USB3 port ***may*** be used.

For filling order see also 3.2 'Feature Fill Order'. The order follows the port prefixes USB0 to USB5. For USB 3.2 SuperSpeed signals the filling order is USB2 to USB3.

At least one USB client port ***should*** be supported. It ***may*** also be available as an OTG port. There can be one or two USB client ports. If only one USB client port is supported, it can be either port 0 or port 3.

USB 3.2 Gen. 1 with 5 Gbit/s is supported. Support for USB 3.2 Gen 2 with 10 Gbit/s might be supported in the future. Limitation for trace length will apply. USB 3.2 Gen. 2 x 2 is not supported.

3.14.1 USB Signal Assignments

	Presence USB 2.0	Presence USB 3.2	OTG/VBUS	Client Capability
USB0	***shall***		***may***	***should***
USB1	***should***			
USB2	***may***	***should***		
USB3	***may***	***may***	***may***	***may***
USB4	***may***			
USB5	***may***			

Table 29: USB Signal Assignments

3.14.2 USB configurations

For the implementation of one or two USB ports the following configurations are allowed depending on the available USB ports on the module and its desired function, as well as USB revision.

In case of more than two available USB ports the feature fill order from chapter 3.2 and allowed USB signal assignment from chapter 3.14.1 must be followed.

Amount of USB ports	USB Revision	USB Function	USB Port
1	***USB2.0***	***Host***	***USB0***
	USB2.0	***Client/OTG***	***USB0***
2	***USB2.0 , USB2.0***	***Host , Host***	***USB0 , USB1***
	USB2.0 , USB2.0	***Client/OTG , Host***	***USB0 , USB1***
	USB2.0 , USB3.2	***Host , Host***	***USB0 , USB2***
	USB2.0 , USB3.2	***Client/OTG , Host***	***USB0 , USB2***

Table 30: USB configurations

3.14.3 USB Signals

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB0+ USB0-	P60 P61	USB Differential Data Pairs for Port 0	I/O USB	USB	Standby		
USB0_EN_OC#	P62	USB Over-Current Sense for Port 0	I/O OD CMOS	3.3V[1]	Standby	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB0_VBUS_DET	P63	USB Port 0 Host Power Detection	I USB VBUS 5V	USB VBUS 5V	Standby		When this Port is used as a device it can be connected to a USB client port VBUS pin.
USB0_OTG_ID	P64	Input Pin to Announce OTG Device Insertion on USB 2.0 Port	I CMOS	3.3V	Standby		
USB1+ USB1-	P65 P66	USB Differential Data Pairs for Port 1	I/O USB	USB	Standby		
USB1_EN_OC#	P67	USB Over-Current Sense for Port 1	I/O OD CMOS	3.3V[1]	Standby	PU 10k	Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB2+ USB2-	P69 P70	USB Differential Data Pairs for Port 2	I/O USB	USB	Standby		
USB2_SSRX+ USB2_SSRX-	S74 S75	Receive Signal Differential Pairs for SuperSpeed on Port 2	I USB SS	USB SS	Standby		DC blocking capacitors 100nF ***shall*** be placed on the Carrier
USB2_SSTX+ USB2_SSTX-	S71 S72	Transmit Signal Differential Pairs for SuperSpeed on Port 2	O USB SS	USB SS	Standby		DC blocking capacitors 100nF ***shall*** be placed on the Module
USB2_EN_OC#	P71	USB Over-Current Sense for Port 2	I/O OD CMOS	3.3V[1]	Standby	PU 10k	Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB3+ USB3-	S68 S69	USB Differential Data Pairs for Port 3	I/O USB	USB	Standby		
USB3_SSRX+ USB3_SSRX-	S65 S66	Receive Signal Differential Pairs for SuperSpeed on Port 3	I USB SS	USB SS	Standby		DC blocking capacitors 100nF ***shall*** be placed on the Carrier
USB3_SSTX+ USB3_SSTX-	S62 S63	Transmit Signal Differential Pairs for SuperSpeed on Port 3	O USB SS	USB SS	Standby		DC blocking capacitors 100nF ***shall*** be placed on the Module

[1] 3.3V or switched 3.3V: if a USB channel is not used, then the USB[0:5]_EN_OC# pull-up rail may be held at GND to prevent leakage currents.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB3_EN_OC#	P74	USB Over-Current Sense for Port 3	I/O OD CMOS	3.3V[1]	Standby	PU 10k	Pulled low by Module OD driver to disable USB3 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB3_VBUS_DET	S37	USB Port 3 Host Power Detection	I USB VBUS 5V	USB VBUS 5V	Standby		when this Port is used as a Device
USB3_OTG_ID	S104	Input Pin to Announce OTG Device Insertion on USB 3.2 Port	I CMOS	3.3V	Standby		
USB4+ USB4-	S35 S36	USB Differential Data Pairs for Port 4	I/O USB	USB	Standby		
USB4_EN_OC#	P76	USB Over-Current Sense for Port 4	I/O OD CMOS	3.3V[1]	Standby	PU 10k	Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB5+ USB5-	S59 S60	USB Differential Data Pairs for Port 5	I/O USB	USB	Standby		
USB5_EN_OC#	S55	USB Over-Current Sense for Port 5	I/O OD CMOS	3.3V[1]	Standby	PU 10k	Pulled low by Module OD driver to disable USB5 power. Pulled low by Carrier OD driver to indicate over-current situation.

Table 31: USB Signals

3.14.4 USB[0:5]_EN_OC# Discussion

The Module USB[0:5]_EN_OC# pins are multi-function Module pins, with a pull-up to a 3.3V rail on the Module, an OD driver on the Module, and, if the OC# (over-current) monitoring function is implemented on the Carrier, an OD driver on the Carrier. The use is as follows:

1) On the Carrier Board, for external plug-in USB peripherals (USB memory sticks, cameras, keyboards, mice, etc.) USB power distribution is typically handled by USB power switches such as the Texas Instruments TPS2052B or the Micrel MIC2026-1 or similar devices. The Carrier implementation is more straightforward if the Carrier USB power switches have active–high power enables and active low open drain OC# outputs (as the TI and Micrel devices referenced do). The USB power switch Enable and OC# pins for a given USB channel are tied together on the Carrier. The USB power switch enable pin must function with a low input current. The TI and Micrel devices referenced above require 1 microampere or less, at a 3.3V enable voltage level.
2) The Module drives USB[0:5]_EN_OC# low to disable the power delivery to the USB[0:5] device.
3) The Module floats USB[0:5]_EN_OC# to enable power delivery. The line is pulled to 3.3V by the Module pull-up, enabling the Carrier Board USB power switch. If there is a USB over-current condition, the Carrier Board USB power switch drives the USB[0:5]_EN_OC# line low. This removes the over-current condition (by disabling the USB switch enable input), and allows Module software to detect the over-current condition. The Module software ***should*** look for a falling edge interrupt on USB[0:5]_EN_OC#, while the port is enabled, to detect the OC# condition. The OC# condition will not last long, as the USB power switch is disabled when the switch IC detects the OC# condition. If the USB power to the port is disabled (USB[0:5]_EN_OC# is driven low by the Module) then the Module software must be aware that the port is disabled, and the low input value on the port does not indicate an over-current condition (because the port power is disabled).If the USB power to the port is disabled, then the Module ***may*** remove the 3.3V pull-up voltage to the USB[0:5]_EN_OC# node, to save the current drain through the pull-up resistor. This is optional and Module design dependent.

Carrier Board USB peripherals that are not removable often do ***not*** make use of USB power switches with current limiting and over-current detection. It is usually deemed un-necessary for non-removable devices. In these cases, the USB[0:5]_EN_OC# pins ***may*** be left unused, or they ***may*** be used as USB[0:5] power enables, without making use of the over-current detect Module input feature.

3.15 PCI Express

The Module ***may*** implement up to four PCIe lanes. The links ***may*** be PCIe Gen 1, 2, 3 or 4, as the Module chip or chipset allows.

The Module PCIe links are primarily PCIe Root Complexes. If the chipset allows it, the PCIe link(s) ***may*** alternatively be configured as a PCIe target(s). This is Module vendor specific.

Modules ***should*** implement the PCIe Link A port. Modules ***may*** implement the PCIe Links B, C and D ports. Fill order is A, B, C then D.

PCIe lanes C and D ***may*** implement SERDES alternatively.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
PCIE_A_TX+ PCIE_A_TX-	P89 P90	Differential PCIe link A transmit data pair	O PCIE		Runtime		Series AC coupled on Module 75-265 nF depending on PCIe generation
PCIE_A_RX+ PCIE_A_RX-	P86 P87	Differential PCIe link A receive data pair	I PCIE		Runtime		Series AC coupled off Module 75-265 nF depending on PCIe generation
PCIE_A_REFCK+ PCIE_A_REFCK-	P83 P84	Differential PCIe Link A reference clock output	O PCIE		Runtime		
PCIE_A_RST#	P75	PCIe Port A reset output	O CMOS	3.3V	Runtime		
PCIE_A_CKREQ#	P78	PCIe Port A clock request	IO OD CMOS	3.3V	Runtime	>10k PU	Can be used for power saving mode on PCIe - Pulled up or terminated on Module
PCIE_B_TX+ PCIE_B_TX-	S90 S91	Differential PCIe link B transmit data pair	O PCIE		Runtime		Series AC coupled on Module 75-265 nF depending on PCIe generation
PCIE_B_RX+ PCIE_B_RX-	S87 S88	Differential PCIe link B receive data pair	I PCIE		Runtime		Series AC coupled off Module 75-265 nF depending on PCIe generation
PCIE_B_REFCK+ PCIE_B_REFCK-	S84 S85	Differential PCIe Link B reference clock output	O PCIE		Runtime		
PCIE_B_RST#	S76	PCIe Port B reset output	O CMOS	3.3V	Runtime		
PCIE_B_CKREQ#	P77	PCIe Port B clock request	IO OD CMOS	3.3V	Runtime	>10k PU	Can be used for power saving mode on PCIe - Pulled up or terminated on Module
PCIE_C_TX+ PCIE_C_TX-	S81 S82	Differential PCIe link C transmit data pair	O PCIE		Runtime		Series AC coupled on Module 75-265 nF depending on PCIe generation
PCIE_C_RX+ PCIE_C_RX-	S78 S79	Differential PCIe link C receive data pair	I PCIE		Runtime		Series AC coupled off Module 75-265 nF depending on PCIe generation
PCIE_C_REFCK+ PCIE_C_REFCK-	P80 P81	Differential PCIe Link C reference clock output	O PCIE		Runtime		
PCIE_C_RST#	S77	PCIe Port C reset output	O CMOS	3.3V	Runtime		
PCIE_D_TX+ PCIE_D_TX-	S29 S30	Differential PCIe link D transmit data pair	O PCIE		Runtime		Series AC coupled on Module 75-265 nF depending on PCIe generation
PCIE_D_RX+ PCIE_D_RX-	S32 S33	Differential PCIe link D receive data pair	I PCIE		Runtime		Series AC coupled off Module 75-265 nF depending on PCIe generation
PCIE_WAKE#	S146	PCIe wake up interrupt to host – common to PCIe links A, B, C, D	I OD CMOS	3.3V	Standby	PU 10k	

Table 32: PCI Express Signals

3.15.1 PCI Express Link Width

A connection between any two PCIe devices is known as a link, and is built up from a collection of one or more lanes. All devices ***shall*** support at least one single lane (x1) link. Devices may optionally support wider links composed of 2 or 4 lanes. Therefore, the root complex ***may*** support different link width additionally to the x1 configuration.

The SMARC specification allows for multiple PCI Express link configurations. Check with the module vendor which configurations are supported.

SMARC 2.1 adds CKREQ# signals for PCIe A and B to allow for enhanced power saving. The clock for PCIe D should be generated from the fixed clock of PCIe C on the carrier.

SMARC PCIe Lane	**Possible Link Configuration**				
PCIe A	x1	x1	x2	x2	x4
PCIe B	x1	x1			
PCIe C	x1	x2	x1	x2	
PCIe D	x1		x1		

Table 33: PCIe Link Configurations

SMARC PCIe Lane	**REFCK and RST Assignments**				
PCIe A	PCIE_A_REFCK PCIE_A_CKREQ# PCIE_A_RST#	PCIE_A_REFCK PCIE_A_CKREQ# PCIE_A_RST#	PCIE_A_REFCK PCIE_A_CKREQ# PCIE_A_RST#	PCIE_A_REFCK PCIE_A_CKREQ# PCIE_A_RST#	PCIE_A_REFCK PCIE_A_CKREQ# PCIE_A_RST#
PCIe B	PCIE_B_REFCK PCIE_B_CKREQ# PCIE_B_RST#	PCIE_B_REFCK PCIE_B_CKREQ# PCIE_B_RST#			
PCIe C	PCIE_C_REFCK PCIE_C_RST#	PCIE_C_REFCK PCIE_C_RST#	PCIE_B_REFCK PCIE_B_CKREQ# PCIE_B_RST#	PCIE_B_REFCK PCIE_B_CKREQ# PCIE_B_RST#	
PCIe D	to be Generated via Buffer from PCIe C Signals		PCIE_C_REFCK PCIE_C_RST#		

Table 34: PCIe Clock and Reset Assignments

3.16 SERDES

SERDES is the general term for SERialized and DESerialized signals on a high-speed differential line. Many chip manufacturers use different functions on the same lines as PCIe and therefore we want to bring this surrogate use to be utilized on the module. The most common use case is here for sure (S)XGMII and therefore the implementation of one or more additional LAN ports. Other functions might also be possible. Of course, these different implementations lead to possible incompatibilities between different modules and a system designer needs to ensure, that this different functionality needs to be available on the regarding module as these are optional features.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SERDES_1_TX+ SERDES_1_TX-	S81 S82	Differential SERDES 1 Transmit Data Pair	O PCIE		Runtime		Series AC coupled on Module[2]
SERDES_1_RX+ SERDES_1_RX-	S78 S79	Differential SERDES 1 Receive Data Pair	I PCIE		Runtime		Series AC coupled on Carrier
SERDES_0_TX+ SERDES_0_TX-	S29 S30	Differential SERDES 0 Transmit Data Pair	O PCIE		Runtime		Series AC coupled on Module
SERDES_0_RX+ SERDES_0_RX-	S32 S33	Differential SERDES 0 Receive Data Pair	I PCIE		Runtime		Series AC coupled on Carrier
MDIO_CLK	S45	MDIO Signals to Configure Possible PHYs	O CMOS	1.8V	Runtime		Signal for communication to a PHY
MDIO_DAT	S46	MDIO Signals to Configure Possible PHYs	I/O OD CMOS	1.8V	Runtime	PU 1k5	Signal for communication to a PHY
SERDES_RST#	S77	SERDES Ports 0/1 reset output	O CMOS	3.3V	Runtime		Signal for resetting the PHYs

Table 35: SERDES Signals

[2] Capacitor values are depending on the module implementation

3.16.1 PCI Express SERDES Pin Sharing

Pin #	PCIE Signal Name	SERDES Signal Name
S81 S82	PCIE_C_TX+ PCIE_C_TX-	SERDES_1_TX+ SERDES_1_TX-
S78 S79	PCIE_C_RX+ PCIE_C_RX-	SERDES_1_RX+ SERDES_1_RX-
P80 P81	PCIE_C_REFCK+ PCIE_C_REFCK-	- -
S77	PCIE_C_RST#	SERDES_RST#[1]
S29 S30	PCIE_D_TX+ PCIE_D_TX-	SERDES_0_TX+ SERDES_0_TX-
S32 S33	PCIE_D_RX+ PCIE_D_RX-	SERDES_0_RX+ SERDES_0_RX-
S45 S46	- -	MDIO_CLK MDIO_DAT

Table 36: PCIe Lane C&D / SERDES Pin Sharing

[1] This signal is only to be implemented, if there is no PCIE_C available on the module. It acts as the reset signal for both SERDES0 and SERDES1.

3.17 SATA

The Module definition allows for one SATA port. The port ***may*** be SATA Gen 1, 2 or 3 as the Modules SOC allows.
The Carrier SATA device ***may*** be selected as the Boot Device – see section Table 45 ‘Control of Boot Sources’ on page 64

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SATA0_TX+ SATA0_TX-	P48 P49	Serial ATA Channel 0 Transmit Output Differential Pair	O SATA		Runtime		Series AC coupled on Module 10 nF
SATA0_RX+ SATA0_RX-	P51 P52	Serial ATA Channel 0 Receive Input Differential Pair	I SATA		Runtime		Series AC coupled on Module 10 nF
SATA_ACT#	S54	SATA Activity Indicator	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current

Table 37: SATA Signals

3.18 Ethernet

The SMARC pin-out supports two multi-gigabit Ethernet capable ports. If only one is implemented, it ***should*** be GBE0.

Additional Ethernet capabilities ***may*** be added by utilizing the optional SERDES (See section 3.16 'SERDES' on page 53 and section 3.16.1 'PCI Express SERDES Pin Sharing' on page 54).

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	P30 P29 P27 P26 P24 P23 P20 P19	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10M/100M/(≥)1G transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/O GBE MDI		Standby		Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in (≥)1G[5], 100M, and 10M bit/sec modes. Some pairs are unused in some modes according to the following: (≥)1G / 100M / 10M MDI0+/- B1_DA+/- / TX+/- / TX+/- MDI1+/- B1_DB+/- / RX+/- / RX+/- MDI2+/- B1_DC+/- MDI3+/- B1_DD+/-
GBE0_LINK_MID#	P21	Link Speed Indication LED for GBE0 lower link speed Previously: GBE0_LINK100#[5]	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current.[3]
GBE0_LINK_MAX#	P22	Link Speed Indication LED for GBE0 maximum link speed Previously: GBE0_LINK1000#[5]	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current.[3]
GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven Low on Link (10M, 100M or (≥)1Gbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current. [3]
GBE0_CTREF	P28	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)	Analog	0 to 3.3V max	Standby		
GBE0_SDP	P6	IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	I/O CMOS	3.3V	Standby		

[3] Needs Carrier based current limiting resistors and LEDs if used. The LED ***may*** be integrated into a Carrier RJ45 jack. A resistor of 68 ohms and a LED with the anode tied to Carrier 3.3V is typical

[5] The operational modes are extended to allow (but not require) multi-gigabit Ethernet operations. The name of the Link Speed indication LED signals have been altered for this purpose. Further information to restrictions and implementation details will be added to the SMARC Design Guide.

GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- GBE1_MDI2+ GBE1_MDI2- GBE1_MDI3+ GBE1_MDI3-	S17 S18 S20 S21 S23 S24 S26 S27	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10M/100M/(≥)1G transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/O GBE MDI		Standby		Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in (≥)1G[6], 100M, and 10M bit/sec modes. Some pairs are unused in some modes according to the following: (≥)1G/ 100M 10M MDI0+/- B1_DA+/- TX+/- TX+/- MDI1+/- B1_DB+/- RX+/- RX+/- MDI2+/- B1_DC+/- MDI3+/- B1_DD+/-
GBE1_LINK_MID#	S19	Link Speed Indication LED for GBE1 lower link speed Previously: GBE1_LINK100#[6]	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current. [3]
GBE1_LINK_MAX#	S22	Link Speed Indication LED for GBE1 maximum link speed Previously: GBE1_LINK1000#[6]	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current. [3]
GBE1_LINK_ACT#	S31	Link / Activity Indication LED Driven Low on Link (10M, 100M or (≥)1Gbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current. [3]
GBE1_CTREF	S28	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)	Analog	0 to 3.3V max	Standby		
GBE1_SDP	P5	IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	I/O CMOS	3.3V	Standby		

Table 38: Ethernet Signals GBE0 and GBE1

[6] The operational modes are extended to allow (but not require) multi-gigabit Ethernet operations. The name of the Link Speed indication LED signals have been altered for this purpose. Further information to restrictions and implementation details will be added to the SMARC Design Guide.

3.19 Watchdog

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
WDT_TIME_OUT#	S145	Watch-Dog-Timer Output, low active	O CMOS	1.8V	Runtime		

Table 39: Watchdog Signals

3.20 GPIO

14 Module pins are allocated for GPIO (general purpose input / output) use. All pins ***should*** be capable of bi-directional operation.

At Module power-up, the state of the GPIO pins ***may not*** be defined, and ***may*** briefly be configured in the "wrong" state, before boot loader code corrects them. Carrier designers ***should*** be aware of this and plan accordingly. Module designers ***should*** generally choose pins that are tri-stated or are inputs during power up and reset, but this ***may not*** always be the case.

All GPIO pins ***should*** be weakly pulled up to 1.8V. If the pull-ups are implemented as discrete resistors, or resistor packs, a value of 470k ***should*** be used. SOC internal pull-up / current source features ***may*** be used instead of external resistors.

All GPIO pins ***shall*** be capable of generating interrupts. The interrupt characteristics (edge or level sensitivity, polarity) are generally configurable in the SOC register set. Inputs with lowest latency interrupts ***should*** be mapped from GPIO6 to GPIO13, where GPIO6 has the lowest latency. GPIO0 to GPIO5 ***may*** have the highest latency. This is important in systems with high time-critical interrupts. Typically, GPI directly connected to SoC have a lower latency than GPIO connected to an I/O expander or some other circuitry that leads to extra latency. If a low latency input signal is needed, like a touch controller interrupt, it is recommended to use GPIO6 and for a 2nd one GPIO7.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO0	P108	GPIO Pin 0 Preferred Output	I/O CMOS	1.8V	Runtime	PU 470k[4]	Alternative use: CAM0_PWR#
GPIO1	P109	GPIO Pin 1 Preferred Output	I/O CMOS	1.8V	Runtime	PU 470k[4]	Alternative use: CAM1_PWR#
GPIO2	P110	GPIO Pin 2 Preferred Output	I/O CMOS	1.8V	Runtime	PU 470k[4]	Alternative use: CAM0_RST#
GPIO3	P111	GPIO Pin 3 Preferred Output	I/O CMOS	1.8V	Runtime	PU 470k[4]	Alternative use: CAM1_RST#
GPIO4	P112	GPIO Pin 4 Preferred Output	I/O CMOS	1.8V	Runtime	PU 470k[4]	Alternative use: HDA_RST#
GPIO5	P113	GPIO Pin 5 Preferred Output	I/O CMOS	1.8V	Runtime	PU 470k[4]	Alternative use: PWM_OUT
GPIO6	P114	GPIO Pin 6 Preferred Input	I/O CMOS	1.8V	Runtime	PU 470k[4]	Alternative use: TACHIN Lowest interrupt latency GPI
GPIO7	P115	GPIO Pin 7 Preferred Input	I/O CMOS	1.8V	Runtime	PU 470k[4]	
GPIO8	P116	GPIO Pin 8 Preferred Input	I/O CMOS	1.8V	Runtime	PU 470k[4]	
GPIO9	P117	GPIO Pin 9 Preferred Input	I/O CMOS	1.8V	Runtime	PU 470k[4]	
GPIO10	P118	GPIO Pin 10 Preferred Input	I/O CMOS	1.8V	Runtime	PU 470k[4]	
GPIO11	P119	GPIO Pin 11 Preferred Input	I/O CMOS	1.8V	Runtime	PU 470k[4]	
GPIO12	S142	GPIO Pin 12 Preferred Input	I/O CMOS	1.8V	Runtime	PU 470k[4]	
GPIO13	S123	GPIO Pin 13 Preferred Input	I/O CMOS	1.8V	Runtime	PU 470k[4]	

Table 40: GPIO Signals

[4] SMARC Spec also allows for SoC integrated Pull-Ups, these can be ≥ 20k. Max 2.2k PD should be implemented on Carrier if a low level needs to be ensured.

3.20.1 Alternative GPIO Pin Usage

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAM0_PWR#	P108	Camera 0 Power Enable, Active Low Output	O CMOS	1.8V	Runtime	PU 470k[6]	
CAM1_PWR#	P109	Camera 1 Power Enable, Active Low Output	O CMOS	1.8V	Runtime	PU 470k[6]	
CAM0_RST#	P110	Camera 0 Reset, Active Low Output	O CMOS	1.8V	Runtime	PU 470k[6]	
CAM1_RST#	P111	Camera 1 Reset, Active Low Output	O CMOS	1.8V	Runtime	PU 470k[6]	
HDA_RST#	P112	HD Audio Reset, Active Low Output	O CMOS	1.8V	Runtime	PU 470k[6]	
PWM_OUT	P113	Fan Speed Control	O CMOS	1.8V	Runtime	PU 470k[6]	Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.
TACHIN	P114	Fan Tachometer Input	I CMOS	1.8V	Runtime	PU 470k[6]	
SERDES0_INT#	P115	SERDES 0 Interrupt, Activ Low Input	I CMOS	1.8V	Runtime	PU 470k[6]	
SERDES1_INT#	P116	SERDES 1 Interrupt, Activ Low Input	I CMOS	1.8V	Runtime	PU 470k[6]	

Table 41: Alternative Use of GPIO Signals

[6] SMARC Spec also allows for SoC integrated Pull-Ups, these can be ≥ 20k. Max 2.2k PD should be implemented on Carrier if a low level needs to be ensured.

3.20.2 GPIO Pin Sharing

Pin #	GPIO Signal Name	Alternative Use
P108	GPIO0	CAM0_PWR#
P109	GPIO1	CAM1_PWR#
P110	GPIO2	CAM0_RST#
P111	GPIO3	CAM1_RST#
P112	GPIO4	HDA_RST#
P113	GPIO5	PWM_OUT
P114	GPIO6	TACHIN
P115	GPIO7	SERDES0_INT#
P116	GPIO8	SERDES1_INT#

Table 42: GPIO Pin Sharing

3.21 Management Pins

The input pins listed in this table are all active low and are meant to be driven by OD (open drain) devices on the Carrier. The Carrier either floats the line or drives it to GND. No Carrier pull-ups are needed. The pull-up functions are performed on the Module. The voltage rail that these lines are pulled to on the Module varies, depending on the design, and ***may*** be anywhere from 1.8V to 5V.

Switches to GND ***may*** be used instead of OD drivers for lines such as PWR_BTN# and RESET_IN#.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BATLOW#	S156	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	1.8 to 5 V	Standby/Sleep	PU 10k	Driven by OD on Carrier.
CARRIER_PWR_ON	S154	Carrier Board circuits (apart from power management and power path circuits) ***should not*** be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	1.8V	Standby/Sleep		On x86 designs this pin should utilize a standby related power signal i.e. RSM_RST# or SLP_A# signal.
CARRIER_STBY#	S153	The Module ***shall*** drive this signal low when the system is in a standby power state.	O CMOS	1.8V	Standby/Sleep		On x86 designs this pin should utilize the SUS_S3# signal.
CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	1.8 to 5 V	Standby/Sleep	PU 10k	Driven by OD on Carrier.
CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	I OD CMOS	1.8 to 5 V	Standby/Sleep	PU 10k	Driven by OD on Carrier.
VIN_PWR_BAD#	S150	Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***shall not*** be enabled while this signal is held low by the Carrier.	I OD CMOS	VDD_IN		PU 10k	Module must implement PU but actual value is depended on particular Module design. Driven by OD on Carrier
SLEEP#	S149	Sleep indicator from Carrier Board. ***May*** be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module.	I OD CMOS	1.8 to 5V	Standby	PU 10k	Driven by OD on Carrier.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module.	I OD CMOS	1.8 to 5 V	Standby	PU 10k	Driven by OD on Carrier.
POWER_BTN#	P128	Power-button input from Carrier Board. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be debounced on the Module.	I OD CMOS	1.8 to 5 V	Standby/Sleep	PU 10k	Driven by OD on Carrier.
RESET_OUT#	P126	General purpose reset output to Carrier Board.	O CMOS	1.8V	Standby		
RESET_IN#	P127	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise. This signal ***Shall*** be level triggered during bootup to allow to stop booting of the module. After bootup it ***May*** act as an edge triggered signal.	I OD CMOS	1.8 to 5 V	Standby	PU 10k	Driven by OD on Carrier.
I2C_PM_DAT	P122	Power management I2C bus DATA	I/O OD CMOS	1.8V	Standby/Sleep	PU 2k2	On x86 systems these serve as SMB DATA.
I2C_PM_CK	P121	Power management I2C bus CLK	I/O OD CMOS	1.8V	Standby/Sleep	PU 2k2	On x86 systems these serve as SMB CLK.
SMB_ALERT#	P1	SMBus Alert# (Interrupt) Signal	I OD CMOS	1.8 to 5 V	Standby/Sleep	PU 2k2	
TEST#	S157	Held Low by Carrier to Invoke Module Vendor Specific Test Functions	I OD CMOS	1.8 to 5 V	Standby/Sleep	PU vendor specific value	Module must implement PU but actual value is depended on particular Module design. Carrier Board should leave this pin floating for normal operation. Driven by OD on Carrier

Table 43: Management Signals

[1]

3.22 Boot Select

Three Module pins allow the Carrier Board user to select from eight possible boot devices. Three are Module devices, and four are Carrier devices, and one is a remote device. The pins ***shall*** be weakly pulled up on the Module and the pin states decoded by Module logic. The Carrier ***shall*** either leave the Module pin Not Connected ("Float" in the table below) or ***shall*** pull the pin to GND, per the second table below.

A "Force Recovery" provision exists, per the pin description below.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BOOT_SEL0# BOOT_SEL1# BOOT_SEL2#	P123 P124 P125	Input straps determine the Module boot device.	I OD CMOS	1.8V	Standby	PU 10k	Driven by OD on Carrier.
FORCE_RECOV#	S155	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.	I OD CMOS	1.8V	Standby	PU 10k	Driven by OD on Carrier.

Table 44: Boot Select Signals

	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eSPI (CS0#)
3	GND	Float	Float	Carrier SPI (CS0#)
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

Table 45: Control of Boot Sources

Note: The boot sources shown above are Module options, and ***may not*** be available on all Module designs.

The definition of “boot” is left to the Module designer. Some designs ***may*** literally implement some or all of the table above, such that the first off-SOC code fetches come from the devices listed above. Alternatively, some designs ***may*** always fetch the first few off-SOC instructions from a fixed device, likely a SPI Flash EEPROM, and then re-direct the execution to another device per the table above.

3.23 Power and GND

See section 6 ‘Module Power’ on page 86 for details on input voltages and power sequencing.

Signal Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage - 3.0V min to 5.25V max	Analog	3.0V to 5.25V			
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Module signal and power return, and GND reference	Analog	Ground			
VDD_RTC	S147	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based lithium cell or super cap.	Analog	2.0V to 3.25V			

Table 46: Power Signals

3.24 JTAG

A CPU JTAG interface ***may*** be implemented on the Module, using a small form factor R/A SMT connector. The JTAG pins are used to allow test equipment and circuit emulators to have access to the Module CPU. The pin-out shown below ***may*** be used:

Signal Name	Pin #	Description	I/O Type	I/O Level	Comments
VDD_JTAG	1	JTAG I/O Voltage (sourced by Module)		1.8 to 3.3V	Voltage level depends on the used SOC. Check implementation details with module vendor. A JTAG adapter might use this voltage to adapt the required JTAG signal levels.
JTAG_TRST#	2	JTAG reset, active low	I CMOS	VDD_JTAG	
JTAG_TMS	3	JTAG mode select	I CMOS	VDD_JTAG	
JTAG_TDO	4	JTAG data out	O CMOS	VDD_JTAG	
JTAG_TDI	5	JTAG data in	I CMOS	VDD_JTAG	
JTAG_TCK	6	JTAG clock	I CMOS	VDD_JTAG	
JTAG_RTCK	7	JTAG return clock	I CMOS	VDD_JTAG	
JTAG_RESET_IN#	8	Pulled high at module	I OD CMOS	VDD_JTAG	
MFG_MODE#	9	Pulled low to allow in-circuit SPI ROM update	I CMOS	VDD_JTAG	Pulled low to allow in-circuit SPI ROM update
GND	10				

Table 47: JTAG Signals

The Module JTAG connector ***may*** be implemented with a JST SH series 1mm pitch R/A wire mount header (JST SM10B-SRSS-TB).
FCI 10051922-1010EHLF, SUNFUN Technology LTDFDS0520-10-11Z, Most Well Technology Corp. MWAFC07-S10-FBA-HFSMARC 2.1JTAG

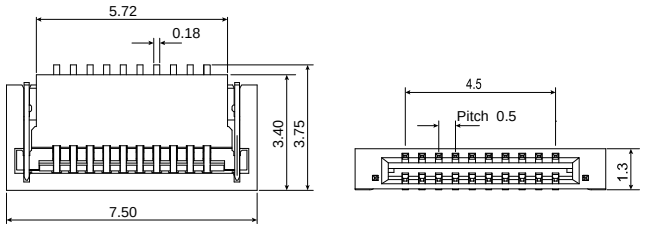


Figure 3: JTAG Connector

3.25 Module Terminations

3.25.1 General

The required Carrier and Module terminations and the component values are described in the signal tables above, although the final decision on specific component values and types is left to the Module designer.

SMARC Module pins of unused features ***may*** be left un-connected.

4 MODULE PIN-OUT MAP

4.1 Module Pin-Out

P-PIN	Primary (Top) Side
P1	SMB_ALERT#
P2	GND
P3	CSI1_CK+
P4	CSI1_CK-
P5	GBE1_SDP
P6	GBE0_SDP
P7	CSI1_RX0+
P8	CSI1_RX0-
P9	GND
P10	CSI1_RX1+
P11	CSI1_RX1-
P12	GND
P13	CSI1_RX2+
P14	CSI1_RX2-
P15	GND
P16	CSI1_RX3+
P17	CSI1_RX3-
P18	GND
P19	GBE0_MDI3-
P20	GBE0_MDI3+
P21	GBE0_LINK_MID#
P22	GBE0_LINK_MAX#
P23	GBE0_MDI2-
P24	GBE0_MDI2+
P25	GBE0_LINK_ACT#
P26	GBE0_MDI1-
P27	GBE0_MDI1+
P28	GBE0_CTREF

S-Pin	Secondary (Bottom) Side
	[5]
S1	CSI1_TX+ / I2C_CAM1_CK
S2	CSI1_TX- / I2C_CAM1_DAT
S3	GND
S4	RSVD
S5	CSI0_TX+ / I2C_CAM0_CK
S6	CAM_MCK
S7	CSI0_TX- / I2C_CAM0_DAT
S8	CSI0_CK+
S9	CSI0_CK-
S10	GND
S11	CSI0_RX0+
S12	CSI0_RX0-
S13	GND
S14	CSI0_RX1+
S15	CSI0_RX1-
S16	GND
S17	GBE1_MDI0+
S18	GBE1_MDI0-
S19	GBE1_LINK_MID#
S20	GBE1_MDI1+
S21	GBE1_MDI1-
S22	GBE1_LINK1_MAX#
S23	GBE1_MDI2+
S24	GBE1_MDI2-
S25	GND
S26	GBE1_MDI3+
S27	GBE1_MDI3-
S28	GBE1_CTREF
S29	PCIE_D_TX+ / SERDES_0_TX+

[5] Shielding should be provided on the Carrier Board close to the Pins S1 and S75 as differential pairs need ground or static signals right and left.

P-PIN	Primary (Top) Side
P29	GBE0_MDI0-
P30	GBE0_MDI0+
P31	SPI0_CS1#
P32	GND
P33	SDIO_WP
P34	SDIO_CMD
P35	SDIO_CD#
P36	SDIO_CK
P37	SDIO_PWR_EN
P38	GND
P39	SDIO_D0
P40	SDIO_D1
P41	SDIO_D2
P42	SDIO_D3
P43	SPI0_CS0#
P44	SPI0_CK
P45	SPI0_DIN
P46	SPI0_DO
P47	GND
P48	SATA_TX+
P49	SATA_TX-
P50	GND
P51	SATA_RX+
P52	SATA_RX-
P53	GND
P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#
P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#
P56	ESPI_CK / SPI1_CK / QSPI_CK
P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1
P58	ESPI_IO_0 / SPI1_DO / QSPI_IO_0
P59	GND
P60	USB0+
P61	USB0-
P62	USB0_EN_OC#
P63	USB0_VBUS_DET
P64	USB0_OTG_ID

S-Pin	Secondary (Bottom) Side
S30	PCIE_D_TX- / SERDES_0_TX-
S31	GBE1_LINK_ACT#
S32	PCIE_D_RX+ / SERDES_0_RX+
S33	PCIE_D_RX- / SERDES_0_RX-
S34	GND
S35	USB4+
S36	USB4-
S37	USB3_VBUS_DET
S38	AUDIO_MCK
S39	I2S0_LRCK
S40	I2S0_SDOUT
S41	I2S0_SDIN
S42	I2S0_CK
S43	ESPI_ALERT0#
S44	ESPI_ALERT1#
S45	MDIO_CLK
S46	MDIO_DAT
S47	GND
S48	I2C_GP_CK
S49	I2C_GP_DAT
S50	HDA_SYNC / I2S2_LRCK / SNDW_CLK1
S51	HDA_SDO / I2S2_SDOUT / SNDW_DAT1
S52	HDA_SDI / I2S2_SDIN / SNDW_DAT0
S53	HDA_CK / I2S2_CK / SNDW_CLK0
S54	SATA_ACT#
S55	USB5_EN_OC#
S56	ESPI_IO_2 / QSPI_IO_2
S57	ESPI_IO_3 / QSPI_IO_3
S58	ESPI_RESET#
S59	USB5+
S60	USB5-
S61	GND
S62	USB3_SSTX+
S63	USB3_SSTX-
S64	GND
S65	USB3_SSRX+

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P65	USB1+	S66	USB3_SSRX-
P66	USB1-	S67	GND
P67	USB1_EN_OC#	S68	USB3+
P68	GND	S69	USB3-
P69	USB2+	S70	GND
P70	USB2-	S71	USB2_SSTX+
P71	USB2_EN_OC#	S72	USB2_SSTX-
P72	RSVD	S73	GND
P73	RSVD	S74	USB2_SSRX+
P74	USB3_EN_OC#	S75	USB2_SSRX-
	Key		***Key***[6]
P75	PCIE_A_RST#	S76	PCIE_B_RST#
P76	USB4_EN_OC#	S77	PCIE_C_RST#
P77	PCIE_B_CKREQ#	S78	PCIE_C_RX+ / SERDES_1_RX+
P78	PCIE_A_CKREQ#	S79	PCIE_C_RX- / SERDES_1_RX-
P79	GND	S80	GND
P80	PCIE_C_REFCK+	S81	PCIE_C_TX+ / SERDES_1_TX+
P81	PCIE_C_REFCK-	S82	PCIE_C_TX- / SERDES_1_TX-
P82	GND	S83	GND
P83	PCIE_A_REFCK+	S84	PCIE_B_REFCK+
P84	PCIE_A_REFCK-	S85	PCIE_B_REFCK-
P85	GND	S86	GND
P86	PCIE_A_RX+	S87	PCIE_B_RX+
P87	PCIE_A_RX-	S88	PCIE_B_RX-
P88	GND	S89	GND
P89	PCIE_A_TX+	S90	PCIE_B_TX+
P90	PCIE_A_TX-	S91	PCIE_B_TX-
P91	GND	S92	GND
P92	HDMI_D2+ / DP1_LANE0+	S93	DP0_LANE0+
P93	HDMI_D2- / DP1_LANE0-	S94	DP0_LANE0-
P94	GND	S95	DP0_AUX_SEL
P95	HDMI_D1+ / DP1_LANE1+	S96	DP0_LANE1+

[6] Shielding should be provided on the Carrier Board close to the Pins S1 and S75 as differential pairs need ground or static signals right and left.

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P96	HDMI_D1- / DP1_LANE1-	S97	DP0_LANE1-
P97	GND	S98	DP0_HPD
P98	HDMI_D0+ / DP1_LANE2+	S99	DP0_LANE2+
P99	HDMI_D0- / DP1_LANE2-	S100	DP0_LANE2-
P100	GND	S101	GND
P101	HDMI_CK+ / DP1_LANE3+	S102	DP0_LANE3+
P102	HDMI_CK- / DP1_LANE3-	S103	DP0_LANE3-
P103	GND	S104	USB3_OTG_ID
P104	HDMI_HPD / DP1_HPD	S105	DP0_AUX+
P105	HDMI_CTRL_CK / DP1_AUX+	S106	DP0_AUX-
P106	HDMI_CTRL_DAT / DP1_AUX-	S107	LCD1_BKLT_EN
P107	DP1_AUX_SEL	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+
P108	GPIO0 / CAM0_PWR#	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-
P109	GPIO1 / CAM1_PWR#	S110	GND
P110	GPIO2 / CAM0_RST#	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+
P111	GPIO3 / CAM1_RST#	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-
P112	GPIO4 / HDA_RST#	S113	eDP1_HPD / DSI1_TE
P113	GPIO5 / PWM_OUT	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+
P114	GPIO6 / TACHIN	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-
P115	GPIO7	S116	LCD1_VDD_EN
P116	GPIO8	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+
P117	GPIO9	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-
P118	GPIO10	S119	GND
P119	GPIO11	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+
P120	GND	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-
P121	I2C_PM_CK	S122	LCD1_BKLT_PWM
P122	I2C_PM_DAT	S123	GPIO13
P123	BOOT_SEL0#	S124	GND
P124	BOOT_SEL1#	S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+
P125	BOOT_SEL2#	S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-
P126	RESET_OUT#	S127	LCD0_BKLT_EN
P127	RESET_IN#	S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+
P128	POWER_BTN#	S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-
P129	SER0_TX	S130	GND
P130	SER0_RX	S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+
P131	SER0_RTS#	S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P132	SER0_CTS#	S133	LCD0_VDD_EN
P133	GND	S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+
P134	SER1_TX	S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-
P135	SER1_RX	S136	GND
P136	SER2_TX	S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+
P137	SER2_RX	S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-
P138	SER2_RTS#	S139	I2C_LCD_CK
P139	SER2_CTS#	S140	I2C_LCD_DAT
P140	SER3_TX	S141	LCD0_BKLT_PWM
P141	SER3_RX	S142	GPIO12
P142	GND	S143	GND
P143	CAN0_TX	S144	eDP0_HPD / DSI0_TE
P144	CAN0_RX	S145	WDT_TIME_OUT#
P145	CAN1_TX	S146	PCIE_WAKE#
P146	CAN1_RX	S147	VDD_RTC
P147	VDD_IN	S148	LID#
P148	VDD_IN	S149	SLEEP#
P149	VDD_IN	S150	VIN_PWR_BAD#
P150	VDD_IN	S151	CHARGING#
P151	VDD_IN	S152	CHARGER_PRSNT#
P152	VDD_IN	S153	CARRIER_STBY#
P153	VDD_IN	S154	CARRIER_PWR_ON
P154	VDD_IN	S155	FORCE_RECOV#
P155	VDD_IN	S156	BATLOW#
P156	VDD_IN	S157	TEST#
		S158	GND

Table 48: Module Pin-Out

5 MECHANICAL DEFINITIONS

5.1 Carrier Connector

The Carrier Board connector is a 314 pin 0.5mm pitch right angle part designed for use with 1.2mm thick mating PCBs with the appropriate edge finger pattern. The connector is commonly used for MXM3 graphics cards. The SMARC Module uses the connector in a way quite different from the MXM3 usage.

Vendor	Vendor P/N	Stack Height	Body Height	Contact Plating	Pin Style	Body Color	Notes
Foxconn	AS0B821-S43B - 7H	1.5mm	4.3mm	Flash	Std	Black	
Foxconn	AS0B826-S43B - 7H	1.5mm	4.3mm	10 u-in	Std	Black	
JAE	MM70-314B2-1-R500	1.5mm	4.3mm	0.1 u-meter	Std	Black	
Aces	91781-314 2 8-001	2.7mm	5.2mm	3 u-in	Std	Black	THT Options available[1]
Foxconn	AS0B821-S55B - 7H	2.7mm	5.5mm	Flash	Std	Black	
Foxconn	AS0B826-S55B - 7H	2.7mm	5.5mm	10 u-in	Std	Black	
JAE	MM70-314B1-2-R300	4.4mm	6.7mm	0.3 u-meter	Std	Black	
Aces	91781-314 0 M-001	5.0mm	7.5mm	3 u-in	Std	Black	THT Options available[1]
Amphenol	10151114-001TLF	5.0mm	7.8mm	30 u-in	Std	Black	
Foxconn	AS0B821-S78B - 7H	5.0mm	7.8mm	Flash	Std	Black	
Foxconn	AS0B826-S78B - 7H	5.0mm	7.8mm	10 u-in	Std	Black	
Yamaichi	CN113-314-2001-VE-TR	5.0mm	7.8mm	0.3 u-meter	Std	Black	Automotive Grade

Table 49: Carrier Connectors

[1] For improved mechanical strength and security there are connector variations available with two additional THT soldering pins. Please check the datasheet of the connectors for specifics and possible deviations.

Other, taller stack heights ***may*** be available from these and other vendors. Stack heights as tall as 11mm are shown on the Aces web site.

Note: Many of the vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for SMARC use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards. The SMARC Module “ungangs” these pins to allow more signal pins. Footprint and pin numbering information for application of this 314 pin connector to SMARC is given in the sections below.

5.2 Connector Pin Numbering Convention

The Module pins are designated as P1 – P156 on the Module Primary (Top) side, and S1 – S158 on the Module Secondary (Bottom) side. There is a total of 314 pins on the Module. The connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key (4 on the primary side and 3 on secondary side).

The Secondary (Bottom) side faces the Carrier Board when a normal or standard Carrier connector is used. Some connector vendors offer “reverse” pin-out connectors, which effectively flip the Module over such that the Module Primary side would face the Carrier Board.

The SMARC Module pins are deliberately numbered as P1 – P156 and S1 – S158 for clarity and to differentiate the SMARC Module from MXM3 graphics Modules, which use the same connector but use the pins for very different functions. MXM3 cards and MXM3 baseboard connectors use a different pin numbering scheme.

5.3 Module Outline – 82x50mm Module

Figure 4 details the 82mm x 50mm Module mechanical attributes, including the pin numbering and edge finger pattern.

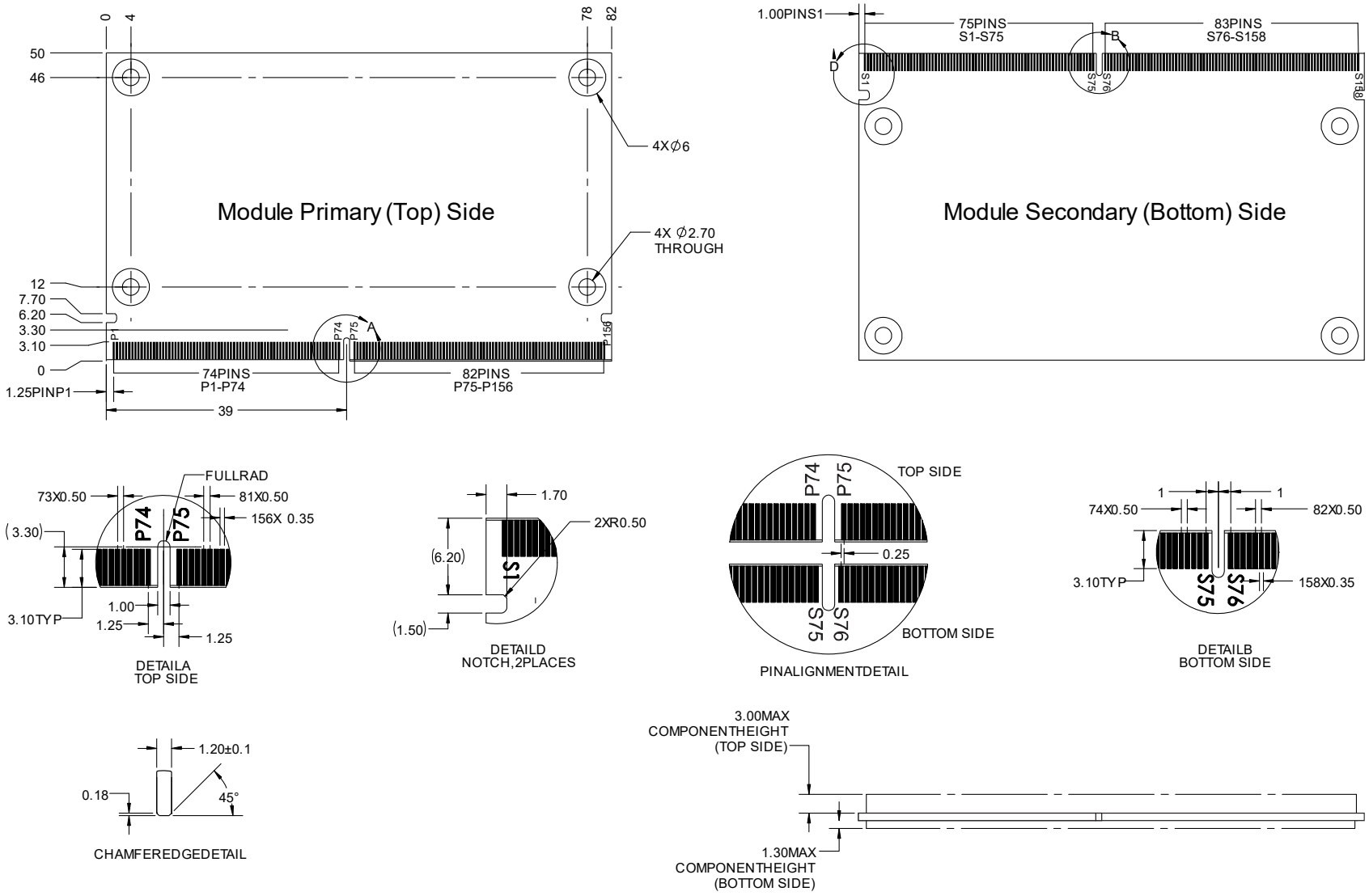


Figure 4: 82x50mm Module Outline

It is recommended that Module components be kept away from the edge fingers, on the top and bottom sides, per the following figure:

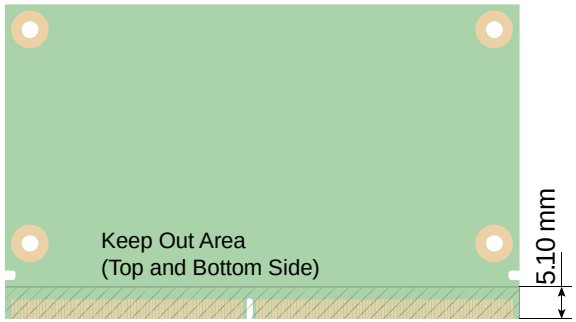


Figure 5: Module Edge Finger Keep Out Area (82x50mm Module)

5.4 Module Outline – 82x80mm Module

The PCB edge finger pattern and spacing details relative to the board edges and lower mounting holes are the same as for the 82mm x 50mm case (see section 5.3 ‘Module Outline – 82x50mm Module’ above), and are not repeated here.

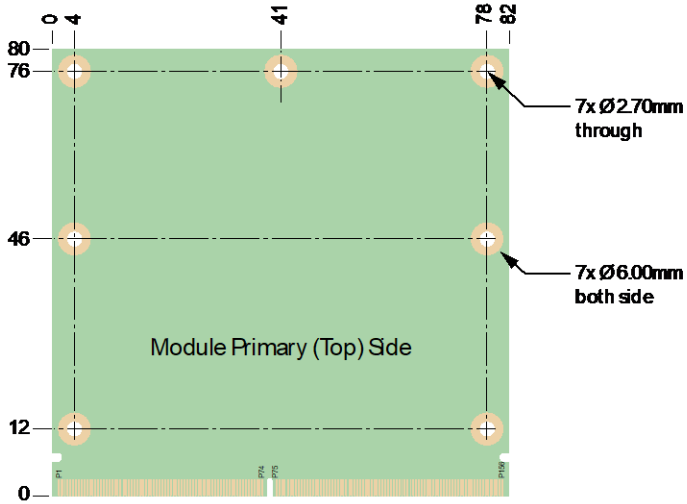


Figure 6: 82x80mm Module Outline

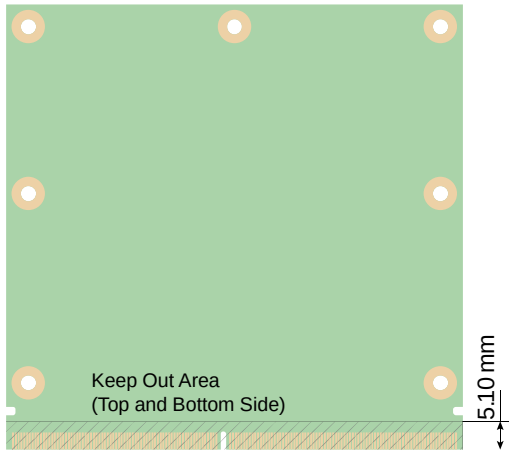


Figure 7: Module Edge Finger Keep Out Area (82x80mm Module)

5.4.1 RF Connector Placement

If onboard wireless technologies are provided the required high frequency antenna connectors ***shall*** be placed at the described positions on the top side of the Modules. If no wireless technologies are provided this position ***may*** be used for other components.

u.FL male connectors ***should*** be used on the Modules. These are miniature RF connectors with an impedance of 50 ohm for antenna applications. U.FL connectors are commonly used for Wi-Fi or GPS in space critical applications. The mated connection is only 2.5 mm high and only requires 3 mm² of board space. u.FL connectors are patented by Hirose but there are many other suppliers offering this connectors.

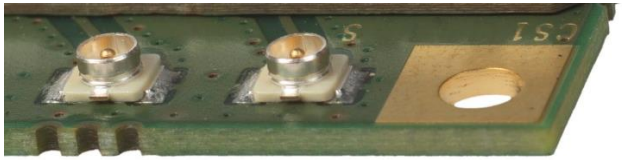


Figure 8: u.FL connector

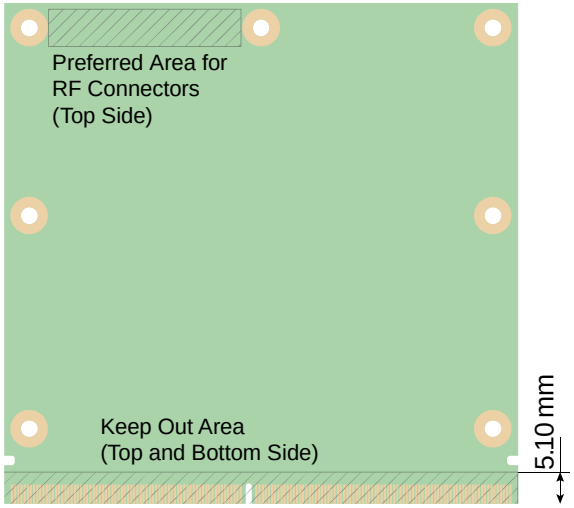


Figure 9: RF connector placement (82x80mm Module)

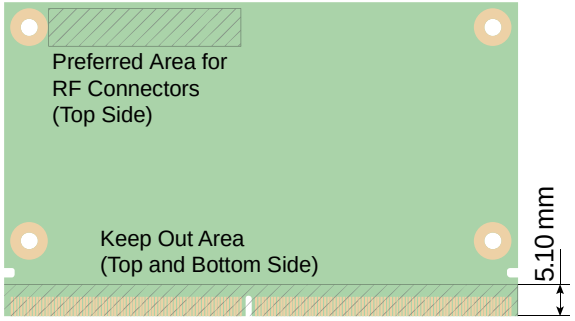


Figure 10: RF connector placement (82x50mm Module)

5.5 Module ‘Z’ Height Considerations

Note from above that the component height on the Module is restricted to a maximum component height of 3mm on the Module Primary (Top) side and to 1.3mm on the Module Secondary (Bottom) side.

The 1.3mm Secondary side component height restriction allows the Module to be used with 1.5mm stack-height Carrier connectors. When used with 1.5mm stack height connectors, the ‘Z’ height profile from Carrier Board Top side to tallest Module component is 5.7mm.

When a 1.5mm stack height Carrier Board connector is used, there ***shall not*** be components on the Carrier Board Top side in the Module region. Additionally, when 1.5mm stack height connectors are used, there ***should not*** be PCB traces on the Carrier top side in the Module shadow. This is to prevent possible problems with metallic Module heat sink attachment hardware that ***may*** protrude through the Module.

If Carrier Board components are required in this region, then the Carrier components must be on the Carrier Bottom side, or a taller Module – to – Carrier connector ***may*** be used. Stack heights of 2.7mm, 3mm, 5mm and up are available.

Not shown in the Figure 11 below are any thermal dissipation components (heat sinks, heat spreaders, etc) nor is fastening hardware (standoffs, spacers, screws, washers, etc) shown. The dimensions of those components must of course be considered in a system design.

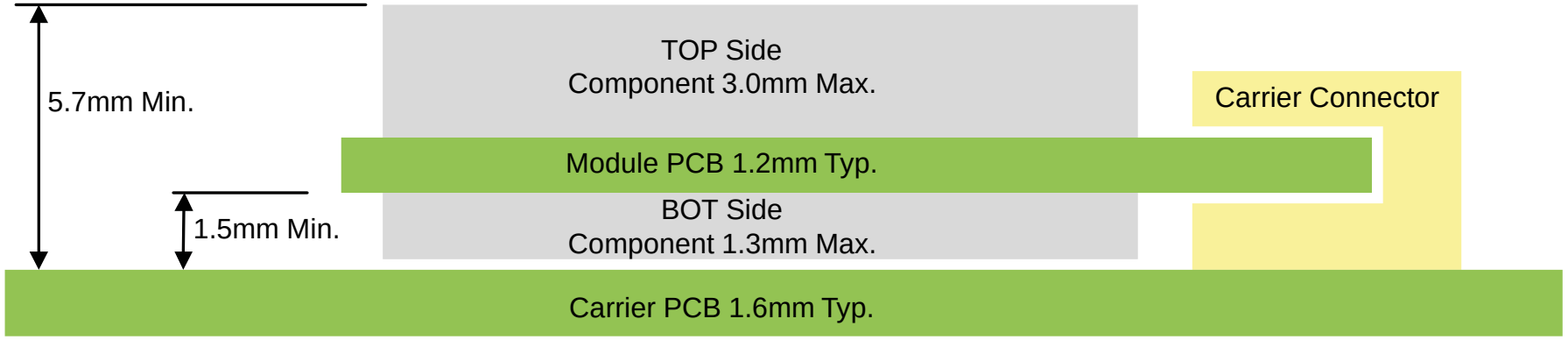


Figure 11: Module Minimum 'Z' Height

Note: There is no clearance defined between heatspreader height and component height. The heatspreader designer, which is usually the module designer has to handle that, e.g. by pockets in the heatspreader.

5.6 Carrier Board Connector PCB Footprint

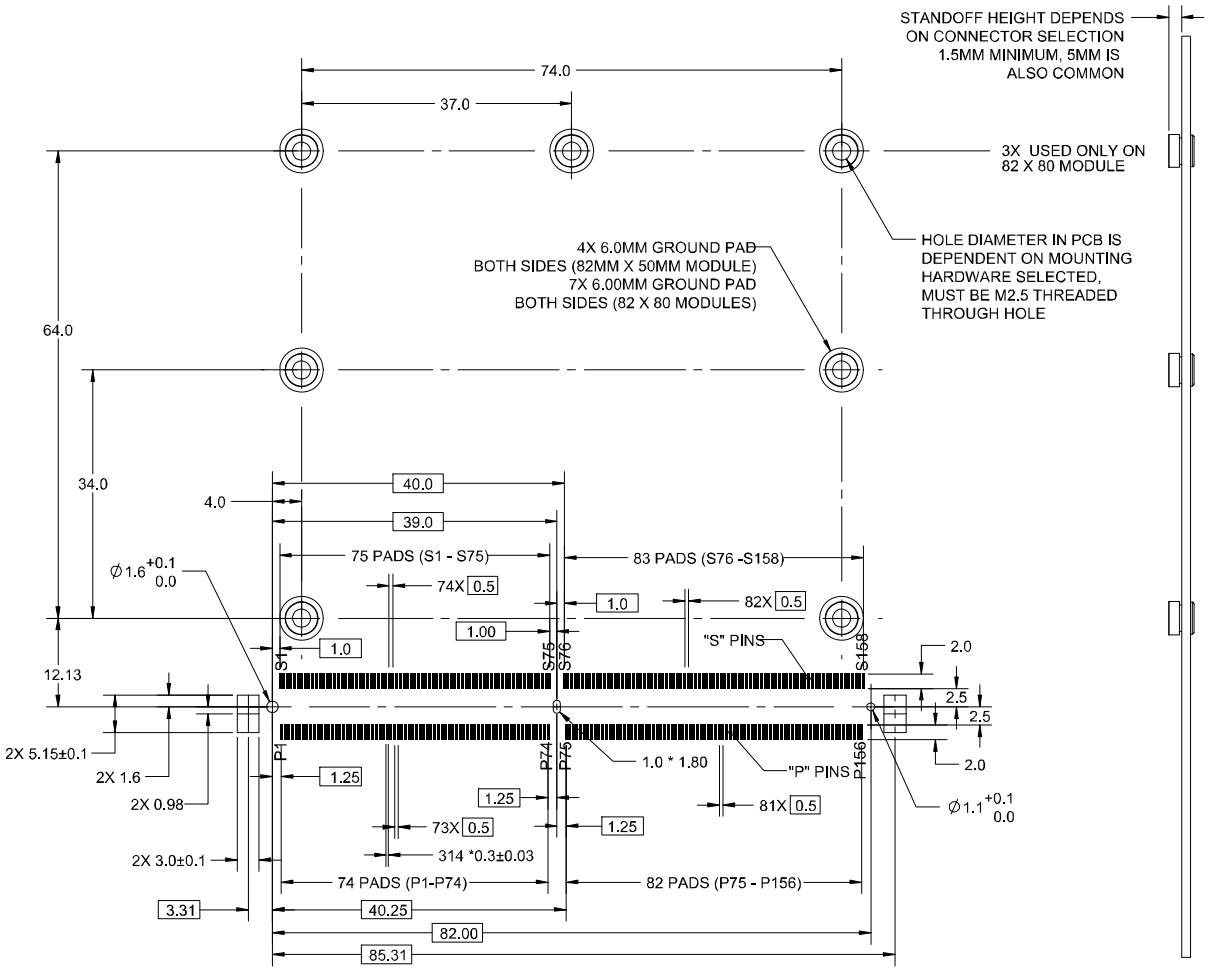


Figure 12: Carrier Board Connector PCB Footprint

Note: The pin numbering shown here is different from the pin numbering used in an MXM3 application. In an SMARC application, all 314 pins of the connector are used individually. The MXM3 power ganging is not used.

Note: The hole diameter for the 4 holes (82mm x 50mm Module) or 7 holes (82mm x 80mm Module) depends on the spacer hardware selection. See the section 5.7 ‘GND Connection’ below for more information.

5.7 GND Connection Mounting Holes

It ***shall*** be possible to tie all Module and Carrier Board mounting holes to GND. The holes ***should*** be tied directly to the GND planes, although Module and Carrier designers ***may*** optionally make the mounting hole GND connections through passive parts, allowing the mounting holes to be isolated from GND if they feel it necessary.

5.8 Carrier Board Standoffs

Standoffs secured to the Carrier Board are expected. The standoffs are to be used with M2.5 hardware. Most implementations will use Carrier Board standoffs that have M2.5 threads (as opposed to clearance holes). A short M2.5 screw and washer, inserted from the Module top side, secures the Module to the Carrier Board threaded standoff.

5.9 Thermal Attachment Points

Attachment points for thermal heat sinks and thermal dissipaters, if needed, are Module design dependent. Thermal hardware ***should*** be attached to the Module using attachment points other than the Module mounting holes (4 mounting holes for the 82mm x 50mm and 7 mounting holes for the 82mm x 80mm Module). The Module mounting holes ***should*** be clear for securing the Module to the Carrier.

Having thermal attachment points separate from the Module mounting holes allows the thermal solution to be shipped with the Module, attached to the Module with thermal interface materials applied, and avoids the disassembly of the thermal interface materials when the end-users places the Module their system. The Module mounting holes ***may*** be used as supplemental thermal attachment points.

5.10 Heat Spreader – 82mm x 50mm Module

A standard heat-spreader plate for use with the SMARC 82mm x 50mm form factor is described below. A standard heat spreader plate definition allows the customer to use a Module from multiple vendors, and the details of the thermal interface to the Module ICs – which can be tricky - becomes the Module designer's problem.

The heat spreader plate is sized at 82mm x 42mm x 3mm, and sits 3mm above the SMARC Module. The heat spreader plate 'Y' dimension is deliberately set at 42mm and not 50mm, to allow the plate to clear the SMARC MXM3 connector. The plate is shown in the Figure 13 below.

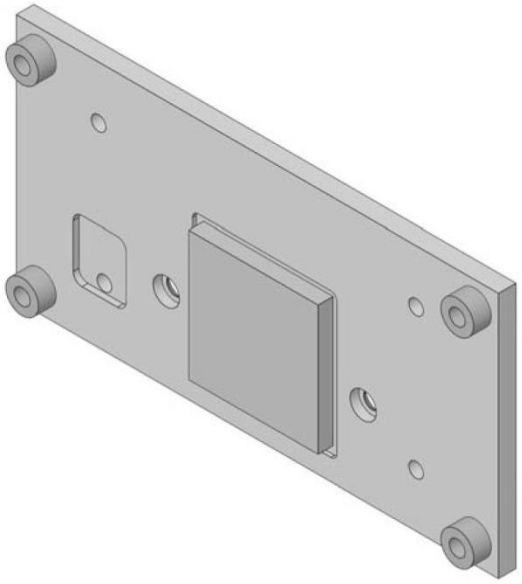


Figure 13: Heat Spreader Isometric View

The internal square in the Figure 13 above is a thermally conductive and mechanically compliant Thermal Interface Material (or "TIM"). The exact X-Y position and Z thickness details of the TIM vary from design to design.

The two holes immediately adjacent to the TIM serve to secure the PCB in the SOC area and compress the TIM.

The four interior holes that are further from the center allow a heat sink to be attached to the heat spreader plate, or they can be used to secure the heat spreader plate to a chassis wall that serves as a heat sink.

Dimensions and further details ***may*** be found in the Figure 14 'Heat Spreader Plan View' on the following page.

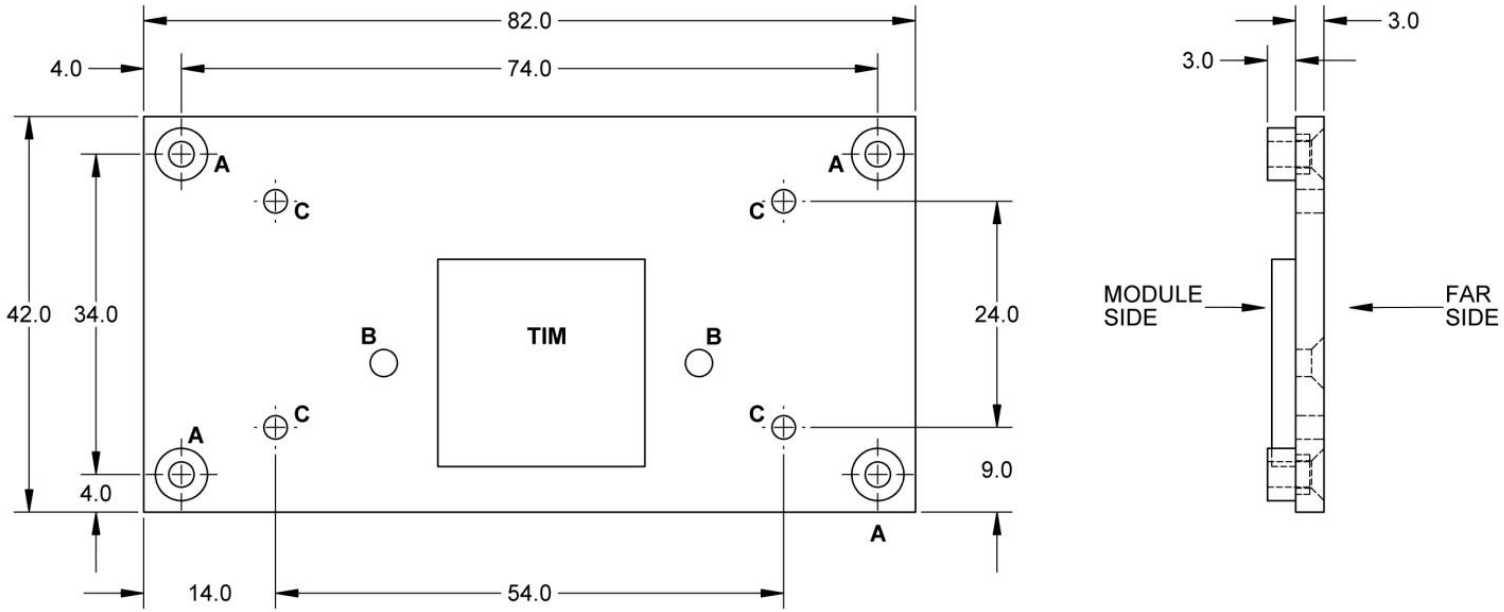


Figure 14: Heat Spreader Plan View

Dimensions in the figure above are in millimeters. "TIM" stands for "Thermal Interface Material". The TIM takes up the small gap between the SOC top and the Module - facing side of the heat spreader.

Hole Reference	Description	Size
A	SMARC Module corner mounting holes Spacing determined by SMARC specification for 82mm x 50mm Modules. Typically, these holes have 3mm length press fit or swaged clearance standoffs on the Module side. These holes are typically countersunk on the far side of the plate, to allow the heat spreader plate to be flush with a secondary heat sink.	Hole size depends on standoffs used. Standoff diameter must be compatible with SMARC Module mounting hole pad and hole size (6.0mm pads, 2.7mm holes on the Module). The holes and standoffs are for use with M2.5 screw hardware. The far side of these holes are counter-sunk to allow the attachment screw to be flush with the far side heat spreader surface.
B	Design – specific attachment points. The X-Y position, size and finish details of these holes ***may*** vary between designs.	Varies, design dependent The far side of these holes are counter-sunk to allow the attachment screw to be flush with the far side heat spreader surface.
C	Fixed location holes to allow the attachment of a heat sink to the heat spreader, or to allow the heat spreader to be secured to a chassis wall that can serve as a heat sink.	M3 threaded holes

Table 50: Heat Spreader Hole Reference

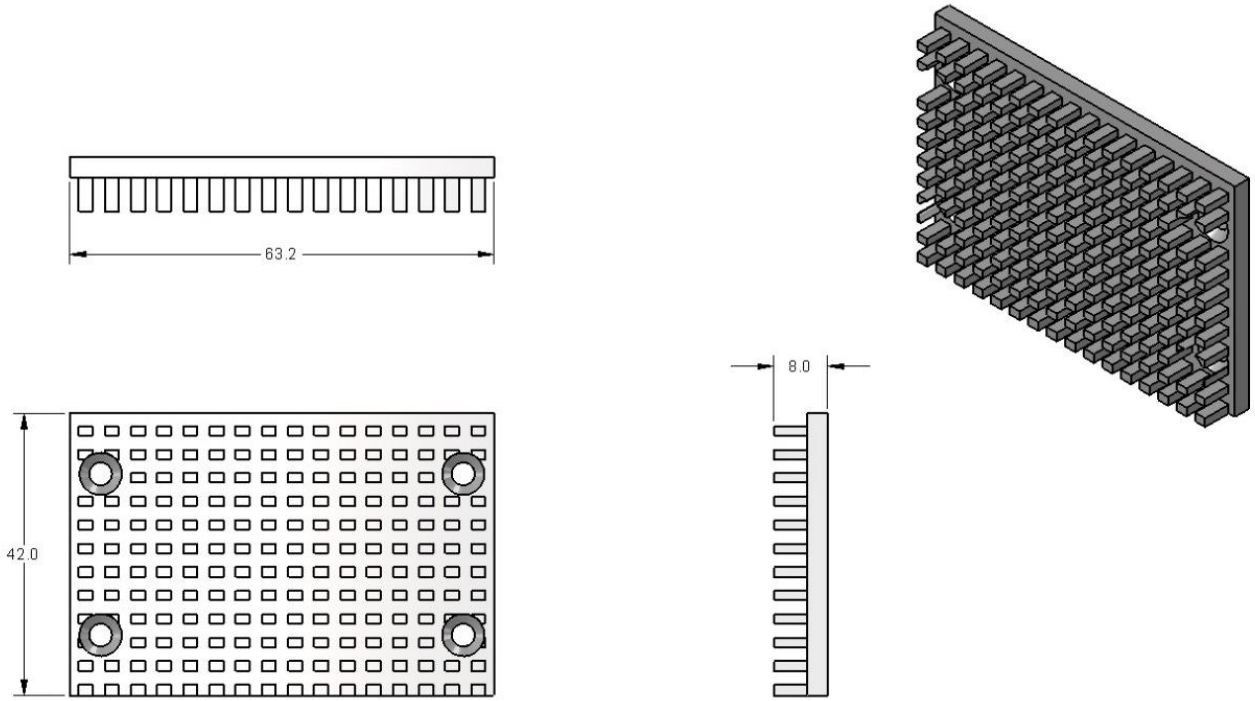


Figure 15: Heat Sink Attachment Option

This figure shows an optional heat sink that can be added on to the heat spreader plate. Some situations ***may*** require a taller heat sink and / or one with an embedded fan. The four holes in the heat sink above are used with M3 flat head screws. The screws engage the 'C' holes in the heat spreader plate in Figure 14 'Heat Spreader Plan View' on the previous page. A relatively large, thin TIM is required between the heat spreader plate "Far Side" and the flat surface of the heat sink.

The heat sink Y dimension matches the 42mm Y dimension of the heat spreader plate. The X dimension of the heat sink is less, at 63.2 mm, than the 82 mm length of the heat spreader plate. This is to allow the heat sink to clear the four Module corner holes (the 'A' holes in Figure 14 'Heat Spreader Plan View'). The heat sink Z dimension can vary according to the thermal situation at hand.

Alternatively, the system enclosure wall ***may*** be used as the heat sink. In this case, the heat spreader plate is secured to the enclosure wall via the four 'C' holes shown in Figure 14 'Heat Spreader Plan View' on the previous page. A large, thin TIM is then required between the heat spreader plate "Far Side" and the enclosure wall.

5.11 Heat Spreader – 82mm x 80mm Module

The heat spreader for an 82mm x 80mm Module is similar to the heat spreader for the 82mm x 50mm Module, but is extended upward by 30mm and appropriate additional holes are provided. The ‘A’ and ‘C’ hole drill details are the same as the ‘A’ and ‘C’ holes on the heat spreader for the 82mm x 50mm Module.

The TIM and the B holes are not fixed, and ***may*** be in locations other than what is shown in Figure 16.

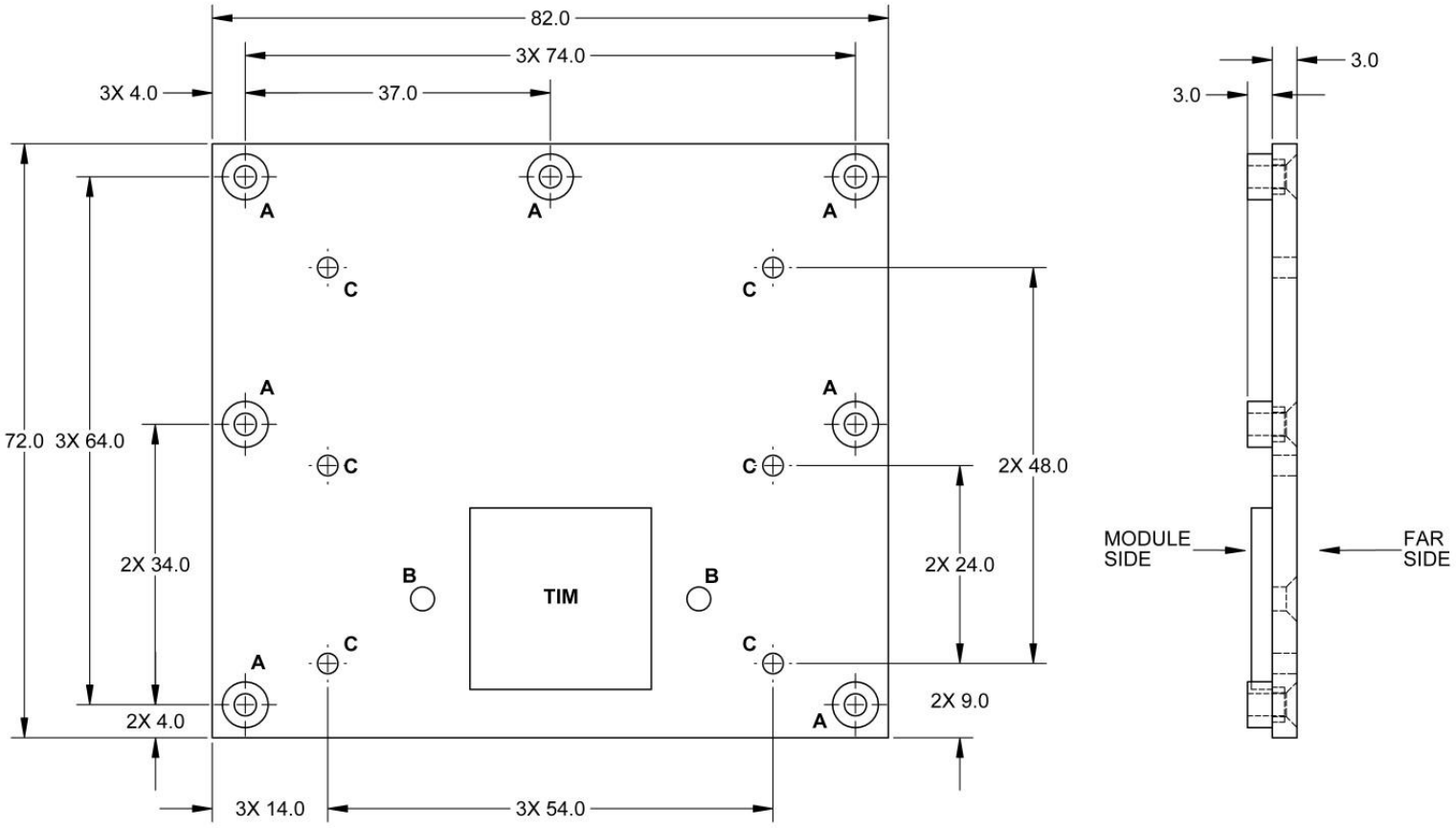


Figure 16: Heat Spreader - 82mm x 80mm Module

5.12 Mechanical Tolerances

The mechanical tolerances of the module have been based on the MXM specification and the tolerances of the MXM 3.0 connector, which is also used for SMARC modules™. The module dimensions and mounting holes of SMARC differ from the MXM specification and the allowed tolerances are defined separately.

For all dimensions which are not defined by the MXM specification, which is mainly applicable for the board contact area of SMARC modules, the ISO 2768-1 shall be applied (e.g. board outline, mounting hole position, cooling solution…). The allowed tolerance class defined in the ISO 2768-1 shall be *f (=fine)*.

6 MODULE POWER

6.1 Input Voltage / Main Power Rail

The Module input power voltage is brought in on the ten VDD_IN pins and returned through the numerous GND pins on the connector.

A Module ***shall*** withstand an indefinite exposure to an applied VDD_IN that ***may*** vary over the 3.0V to 5.25V range, without damage.

A Module ***should*** operate over the entire VDD_IN range of 3.0V to 5.25V.

Modules that use higher wattage SOCs ***may*** be designed to operate with a fixed 5V supply (4.75V to 5.25V).

Modules that are designed for rock-bottom cost and that use low power SOCs ***may*** be designed to operate with a fixed 3.3V supply (3.1V to 3.4V). They ***shall not*** be damaged in any way by exposure to the allowable VDD_IN range of 3.0 to 5.25V.

Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins. At the lowest allowed Module input voltage of 3.0V, this would allow up to 15W of electrical power to be brought in (with no de-rating on the connector current capability). With a 40% connector current de-rating, up to 9W ***may*** be brought in at 3.0V.

If the fixed 5V input option is used, then 25W ***may*** be brought in over the 10 power pins (no de-rating). With a 40% connector de-rating, 15W are allowed to be brought in at 5V.

As a practical matter, ARM most Module designs are expected to be 6W or less. X86 designs are expected to be in the 5W to 12W range, depending on the CPU SKU.

6.2 No Separate Standby Voltage

There is no separate voltage rail for standby power, other than the very low current (optional) RTC voltage rail. All Module operating and standby power comes from the single set of VDD_IN pins. This suits battery power sources well, and is also easy to use with non-battery sources.

6.3 RTC Voltage Rail

RTC backup power ***may*** brought in on the VDD_RTC rail. The RTC consumption is typically 15 µA or less. The allowable VDD_RTC voltage range ***shall*** be 2.0V to 3.25V. The VDD_RTC rail ***may*** be sourced from a Carrier based Lithium cell or Super Cap, or it ***may*** be left open if the RTC backup functions are not required. The Module ***shall*** be able to boot without an external VDD_RTC voltage source.

Important: Lithium cells must be protected against charging by reverse currents, with a series Schottky diode and resistor. It is impractical to have the series diode on the Module, as this complicates the use of Super Caps (they need to be charged, over the Module VDD_RTC pin).

Lithium cells, if used, ***shall*** be protected against charging by a Carrier Schottky diode. The diode is placed in series with the positive battery terminal. The diode anode is on the battery side, and the cathode on the Module VDD_RTC side.

Note that if a Super cap is used, current ***may*** flow out of the Module VDD_RTC rail to charge the Super Cap.

The supply voltage rail used for the Module is VDD_IN. There are no timing relations between this Module supply rail and the optional VDD_RTC.

6.4 Power Rail Definition

The intention of mapping the SMARC Module connector signals to separate power domains is to enable a compatible implementation of power saving sleep state called ***standby state*** between different Module vendors and CPU technologies. At ***runtime state***, all supported IO signals are powered and driven. At ***standby state***, dedicated wake sources ***shall*** be enabled with active interfaces and signals.

Standby state and runtime state are corresponding to the in the x86 world well known ACPI system states Standby and Full On.

If a power saving ***standby state*** is implemented at the Carrier Board and supported by the Module, the IO voltage rails of the Carrier Board are controlled by the Module using the two signals CARRIER_PWR_ON and CARRIER_STBY#. The signal CARRIER_PWR_ON enables the IO supply rails that are powered in ***standby mode***. The signal CARRIER_STBY# enables the additional IO supply rails that are powered in ***runtime mode***.

Comparing to previous releases of SMARC standard, a new low power consumption domain is defined as "Sleep". This is an optional domain which can be used to support DeepSleep states of modern CPU architectures. Typical wake event is the power button only. Optionally the battery management can be used. If the state is not used, Sleep power domain can be tied to Standby domain.

SMARC domain name	ACPI domain name	ACPI System-State	VIN_PWR_BAD#	CARRIER_PWR_ON	CARRIER_STB#	Corresponding Signal for x86 Designs (only for Module designer)
Off			0	0	0	
Sleep	Deep sleep	Pseudo G3 (after Mechanical OFF G3; before Standby)	1	0	0	SLP_SUS# asserted Note: VIN_PWR_BAD# is not tied to SLP_SUS#
Standby	Standby	S5-S3	1	1	0	Standby related power signal i.e. RSMRST# or SLP_SUS# deasserted
Runtime	Full-On	S0	1	1	1	i.e. SLP_S3# deasserted

Table 51: Power Rail Definitions

In order to avoid back driving between module and carrier by high active signals in standby state the signal power domains in the pin description in chapter 3 shall be observed. In general, it is recommended to adapt the Carrier Board power rails to the Module power rails. In some cases, you ***may*** drive signals low or to use weak pull up resistors to minimize back driving. The Carrier Board shall avoid back driving from Module into unpowered circuit at ***standby mode***. The Carrier Board ***shall not*** drive any runtime signals high during ***standby mode***.

Special attention has to be spent at runtime powered output signals in ***standby mode***. SMARC 2.0 modules may have used different signal to power domain assertion. The module datasheet has to be checked for standby mode implementation details to prevent backdriving and to define wakeup sources.

6.5 Power Sequencing

Basically, VDD_IN is the first power domain to be turned on by the carrier circuit during power-up. Other circuit components on the carrier, which are galvanically coupled to the module, shall not be supplied to avoid feedback. From the moment VDD_IN is stable - recognizable by VIN_PWR_BAD# deasserted - the module takes over control of the power sequencing. As soon as the module reaches the next system state standby, CARRIER_PWR_ON signals the carrier to switch on all its standby voltages. No feedback is provided to allow the carrier to signal Power OK to the modules power state machine. When the state Runtime is reached, the module deasserts CARRIER_STBY#. The carrier then switches on the remaining rails.

The following sections 6.5.1 to 6.5.4 show power sequence scenarios with/without sleep power domain and with/without power button.

6.5.1 Power up sequence scenario 1

Power up with sleep power domain and PWR_BTN#.

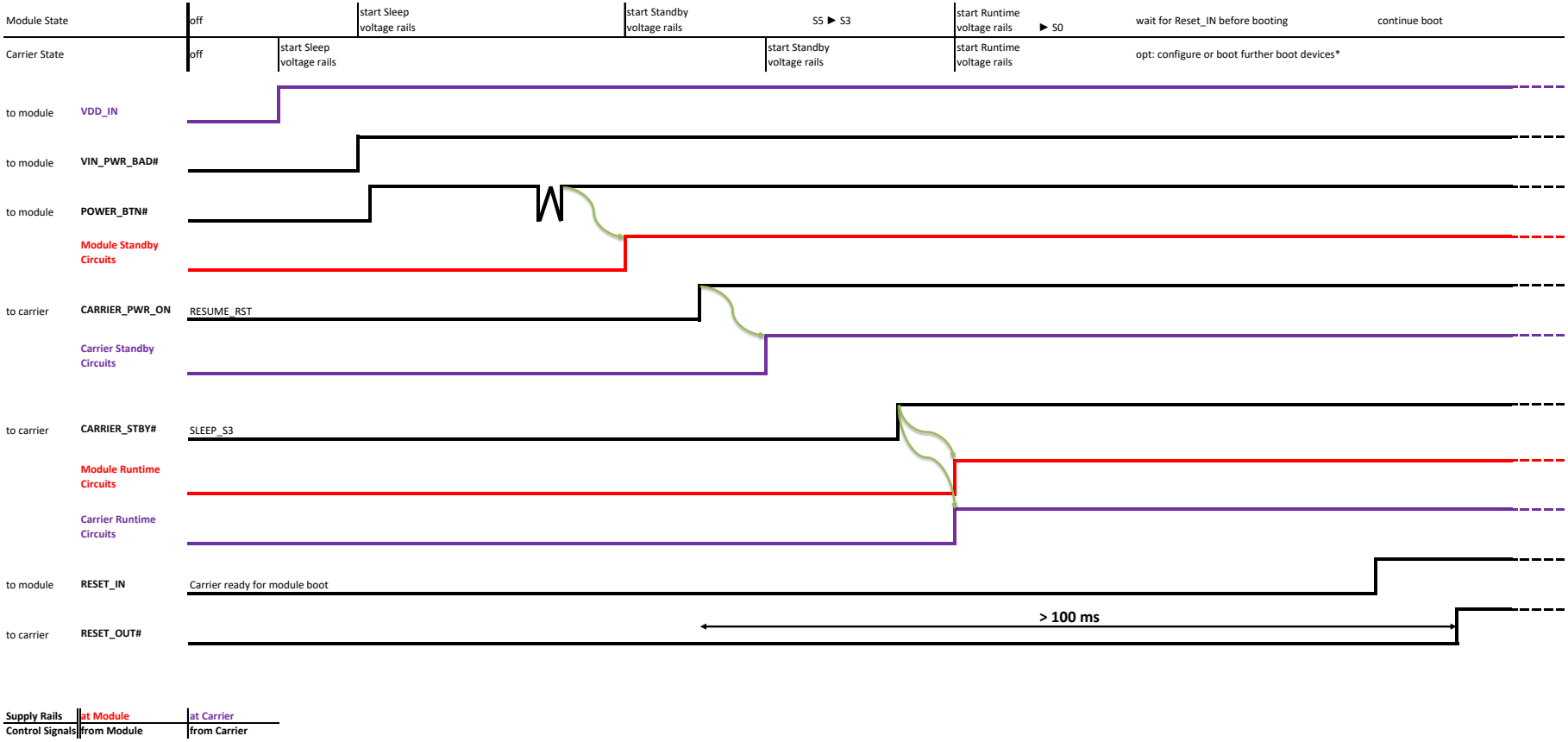


Figure 17: Power sequence diagram sleep and power button

6.5.2 Power up sequence scenario 2

Power up sequence with sleep power domain without PWR_BTN#

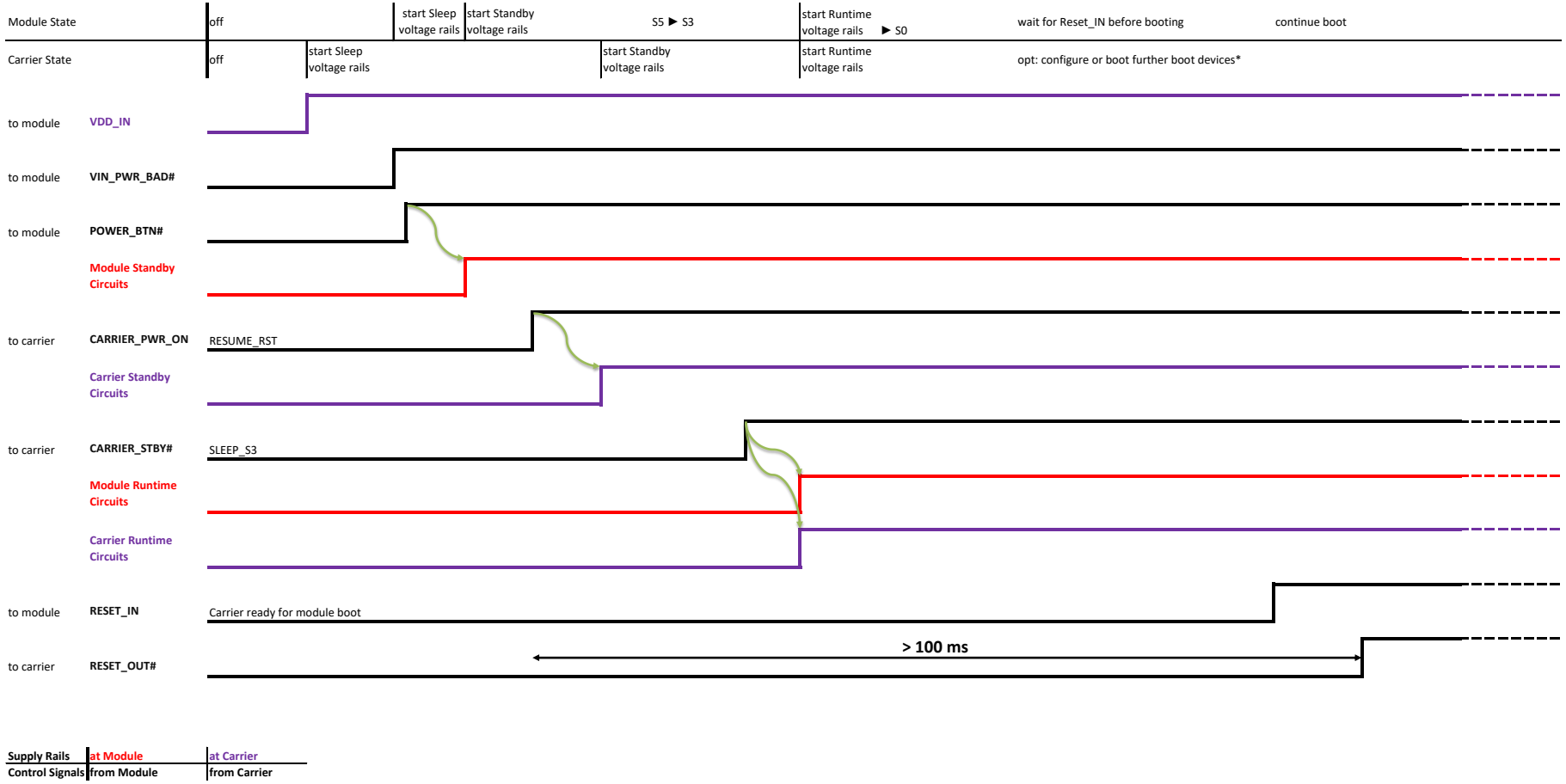


Figure 18: Power sequence diagram sleep, no power button

6.5.3 Power up sequence scenario 3

Power up sequence without sleep power domain and with PWR_BTN#

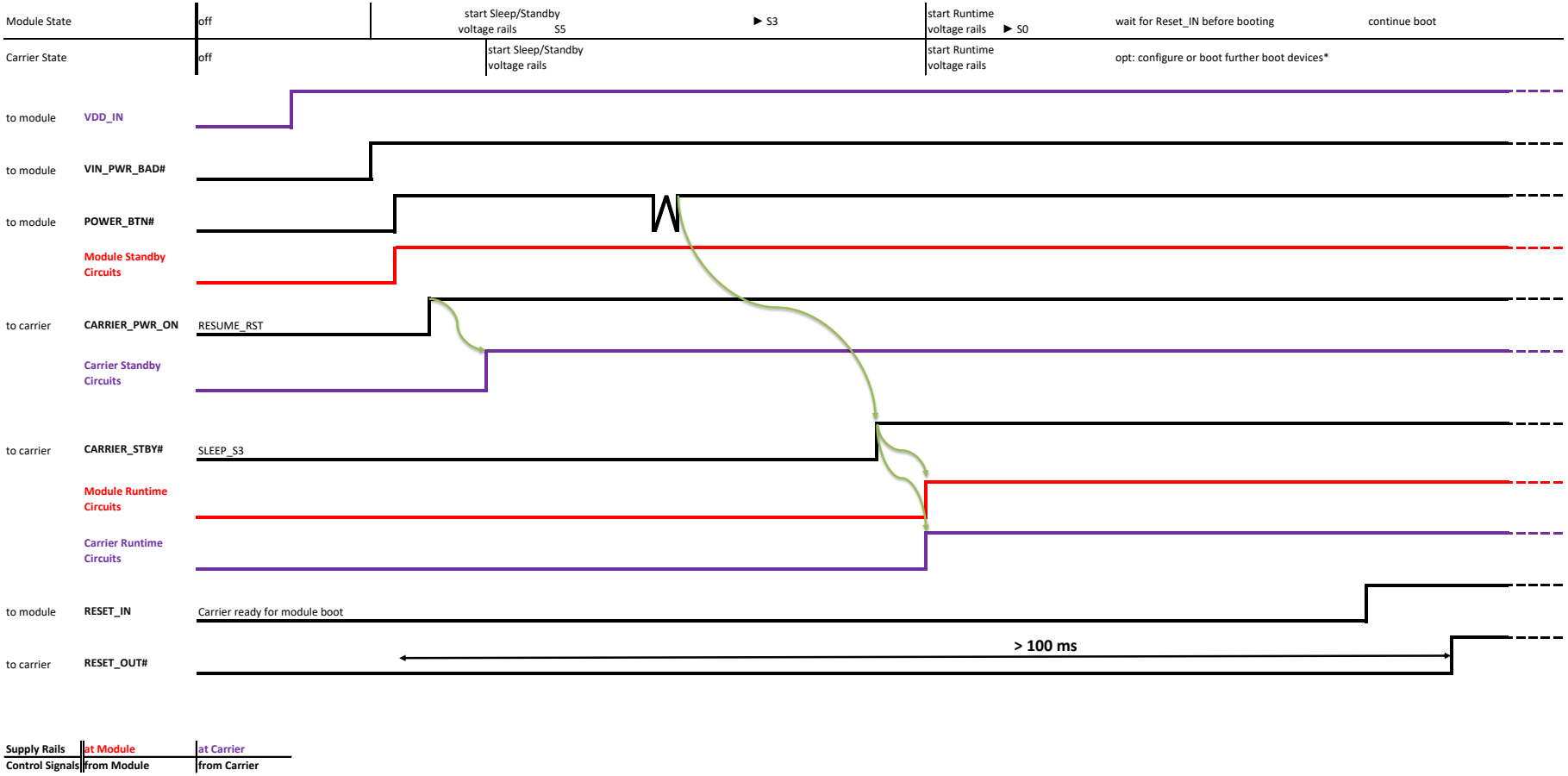


Figure 19: Power sequence diagram power button

6.5.4 Power up sequence scenario 4

Power up sequence without sleep power domain and without PWR_BTN#

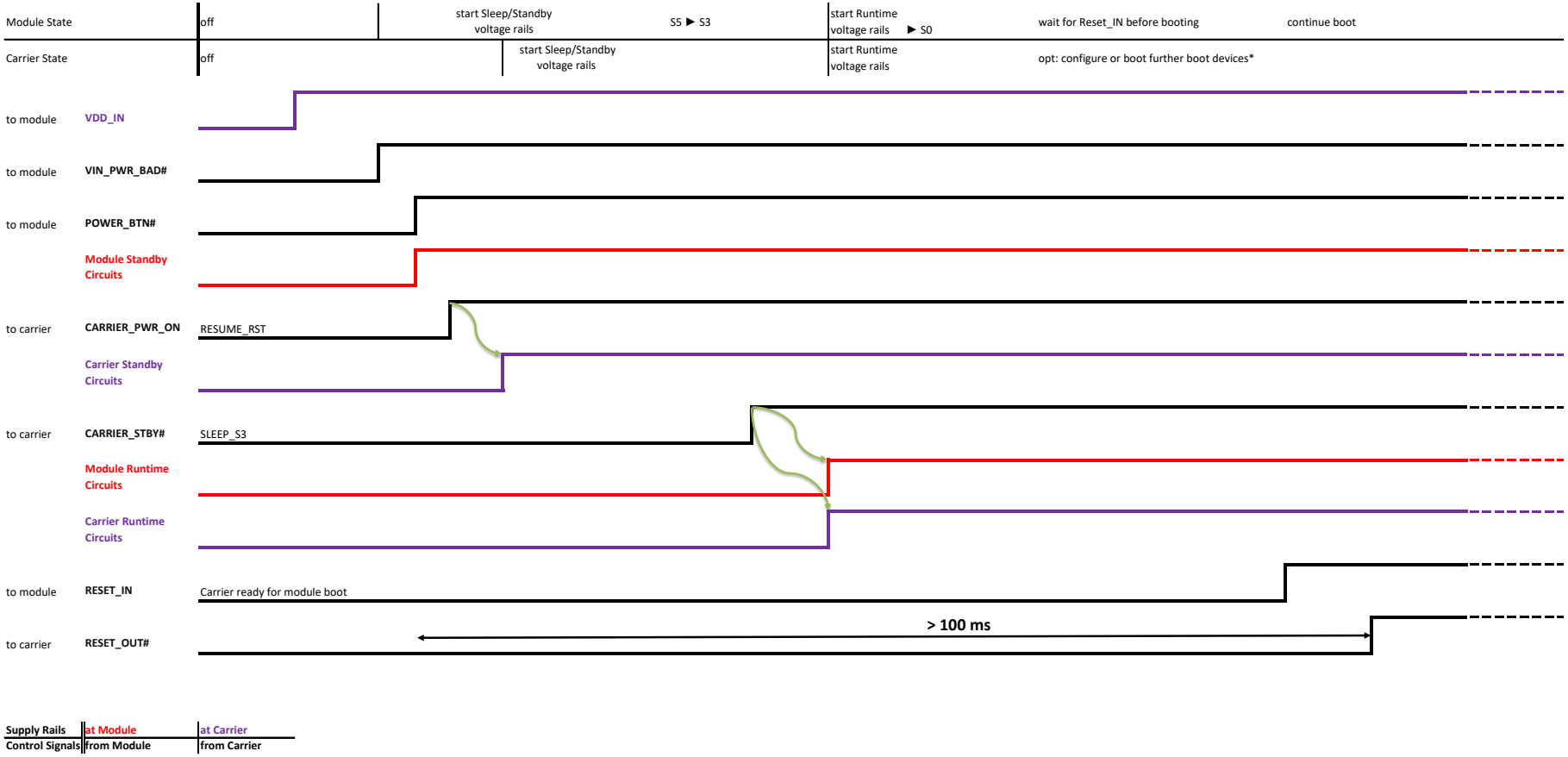


Figure 20: Power sequence diagram, no power button

7 MODULE AND CARRIER SERIAL EEPROMS

SMARC Modules ***should*** include an I2C serial EEPROM on the Module I2C_GP bus. The device used ***should*** be an Atmel 24C32 or equivalent. The device ***shall*** operate at 1.8V. The Module serial EEPROM ***should*** be placed at I2C slave addresses A2 A1 A0 set to 0 (I2C slave address 50 hex, 7 bit address format or A0 / A1 hex, 8 bit format) (recall that for I2C EEPROMs, address bits A6 A5 A4 A3 are set to binary 1010 convention).

The Module serial EEPROM is intended to retain Module parameter information, including a Module serial number. The Module serial EEPROM data structure ***should*** conform to the ***PICMG® EEEP Embedded EEPROM Specification***.

SMARC Carriers ***may*** include an I2C serial EEPROM on the I2C_PM bus, in the Module power domain. The device used ***should*** be an Atmel 24C32 or equivalent. The device ***shall*** operate at 1.8V. The Carrier serial EEPROM ***should*** be placed with I2C slave addresses A2 A1 A0 set to binary 111 (I2C slave address 57 hex, 7 bit address format or AE / AF hex, 8 bit format).

The Carrier serial EEPROM is intended to retain Carrier parameter information. The Carrier serial EEPROM data structure ***should*** conform to the ***PICMG® EEEP Embedded EEPROM Specification***.

8 APPENDIX A: LVDS LCD COLOR MAPPINGS

8.1 LVDS LCD Color Mappings

For flat panel use, parallel LCD data and control information (Red, green and blue color data; Display Enable, Vertical Synch, Horizontal Synch) are commonly serialized onto a set of LVDS differential pairs. The information is packed into frames that are 7 bits long. For 18 bit color depths, the data and control information utilize three LVDS channels (18 data bits + 3 control bits = 21 bits; hence 3 channels with 7 bit frames) plus a clock pair. For 24 bit color depths, four LVDS channels are used (24 data bits + 3 control bits + 1 unused bit = 28 bits, or 4 x 7) plus a clock pair.

The LVDS clock is transmitted as a separate LVDS pair. The LVDS clock period is 7 times longer than the pixel clock period. The LVDS clock edges are off from the 7 bit frame boundaries by 2 pixel periods.

Unfortunately, there are two different 24 bit color mappings in use. The more common one, sometimes referred to as “24 bit standard color mapping”, is not compatible with 18 bit panels, as it places the most significant RGB color data on the 4th LVDS data pair – the pair that is not used on 18 bit panels. There is a less common “24 bit / 18 bit compatible” mapping that puts the least significant color bits of the 24 bit set onto the 4th LVDS pair.

Some panels have pin straps that allow the user to select which color mapping is to be used.

8.1.1 Single Channel Color Mapping

8.1.1.1 General Information

LVDS Channel	Transmit Bit Order	18 Bit Standard	24 Bit / 18 Bit Compatible	24 Bit Standard
0	1	G0	G0	G2
	2	R5	R5	R7
	3	R4	R4	R6
	4	R3	R3	R5
	5	R2	R2	R4
	6	R1	R1	R3
	7	R0	R0	R2
1	1	B1	B1	B3
	2	B0	B0	B2
	3	G5	G5	G7
	4	G4	G4	G6
	5	G3	G3	G5
	6	G2	G2	G4
	7	G1	G1	G3
2	1	DE	DE	DE
	2	VS	VS	VS
	3	HS	HS	HS
	4	B5	B5	B7
	5	B4	B4	B6
	6	B3	B3	B5
	7	B2	B2	B4
3	1	<not used>	<not used>	<not used>
	2	<not used>	B7	B1
	3	<not used>	B6	B0
	4	<not used>	G7	G1
	5	<not used>	G6	G0
	6	<not used>	R7	R1
	7	<not used>	R6	R0

Table 52: LVDS Color Mapping

9 APPENDIX B: DOCUMENT CHANGES

9.1 Changes V1.1 to V2.0

Removed Interfaces

- Parallel camera interface
- Parallel Display interface
- PCI Express presence and clock request signals
- Alternate function block
- SPDIF
- eMMC
- 1 of 3 I2S

Added Interfaces

- 2nd channel LVDS
- 2nd Ethernet
- IEEE1588 trigger signals (software definable pins)
- 4th PCI Express lane
- Extra USB ports (6x USB 2.0 + 2x USB SS signals now)
- x86 power management signals
- eSPI
- DP++

Total Video Interfaces now

- 2x 24 Bit LVDS / eDP 4 channel / MIPI DSI 4 channel
- HDMI / DP++
- DP++

Other Changes

- Added RF connector option
- Changed Module EEPROM from I2C_PM to I2C_GP
- Added power sequencing details
- See detailed pinout changes is section ‘Corrected power-domain for PWR_BTN#, CARRIER_PWR_ON, CARRIER_STBY# signals
- Pinout Comparison’ below
- Some mandatory and optional features changed, see section 3.1 ‘Required and Optional Feature Table’ on page 14

9.2 Changes V2.0 to V2.1

- Incorporated Errata 1.1 Rev. 2 (2/9/2017)
- Updated signal tables
  - Added pin number
  - Added power domain
  - Updated content
  - Added termination information
- Added details for eDP[0:1]_HPD
- Added SERDES as alternative function for PCIeC and PCIeD
- Added MDIO Interface
- Updated power domains and power sequencing
- Added two extra GPIOs
- PCIe Clock Request signals for PCIeA and PCIeB at previous locations
- Changed fill order for MIPI CSI (CSI1 first, then CSI0)
- Added CSI 2 and 3 on extra optional connector
- USB client mode defined more clearly
- Added sleep power domain
- Redefined JTAG connector

9.3 Changes V2.1 to V2.1.1

- Removed wrong AC coupling comment in section 3.5.1 HDMI

9.4 Changes V2.1.1 to V2.2

- Added Soundwire as alternative function for I2S2
- Added SERDES reset signal as alternative function of PCIe reset signal
- Added SERDES interrupt signals as dual-function on GPIO[7:8]
- Updated supported Ethernet speed and renamed the LINK signals accordingly
- Added details for mechanical tolerances
- Updated filling-order for USB and further specified allowed configurations
- Updated GPIOs with filling-order for interrupt latency
- Updated overview of Carrier connectors
- Added filling-order for SPI Chip-Select signals
- Updated support of PCIe up-to Gen 4
- Corrected power-domain for PWR_BTN#, CARRIER_PWR_ON, CARRIER_STBY# signals

9.5 Pinout Comparison

Pin	SMARC 1.1	SMARC 2.0	SMARC 2.1	SMARC 2.2
P1	~~PCAM_PXL_CK1~~	SMB_ALERT_1V8#	SMB_ALERT#	SMB_ALERT#
P2	GND	GND	GND	GND
P3	CSI1_CK+ ~~/ PCAM_D0~~	CSI1_CK+	CSI1_CK+	CSI1_CK+
P4	CSI1_CK- ~~/ PCAM_D1~~	CSI1_CK-	CSI1_CK-	CSI1_CK-
P5	~~PCAM_DE~~	GBE1_SDP	GBE1_SDP	GBE1_SDP
P6	~~PCAM_MCK~~	GBE0_SDP	GBE0_SDP	GBE0_SDP
P7	CSI1_D0+ ~~/ PCAM_D2~~	CSI1_RX0+	CSI1_RX0+	CSI1_RX0+
P8	CSI1_D0- ~~/ PCAM_D3~~	CSI1_RX0-	CSI1_RX0-	CSI1_RX0-
P9	GND	GND	GND	GND
P10	CSI1_D1+ ~~/ PCAM_D4~~	CSI1_RX1+	CSI1_RX1+	CSI1_RX1+
P11	CSI1_D1- ~~/ PCAM_D5~~	CSI1_RX1-	CSI1_RX1-	CSI1_RX1-
P12	GND	GND	GND	GND
P13	CSI1_D2+ ~~/ PCAM_D6~~	CSI1_RX2+	CSI1_RX2+	CSI1_RX2+
P14	CSI1_D2- ~~/ PCAM_D7~~	CSI1_RX2-	CSI1_RX2-	CSI1_RX2-
P15	GND	GND	GND	GND
P16	CSI1_D3+ ~~/ PCAM_D8~~	CSI1_RX3+	CSI1_RX3+	CSI1_RX3+
P17	CSI1_D3- ~~/ PCAM_D9~~	CSI1_RX3-	CSI1_RX3-	CSI1_RX3-
P18	GND	GND	GND	GND
P19	GBE_MDI3-	GBE0_MDI3-	GBE0_MDI3-	GBE0_MDI3-
P20	GBE_MDI3+	GBE0_MDI3+	GBE0_MDI3+	GBE0_MDI3+
P21	GBE_LINK100#	GBE0_LINK100#	GBE0_LINK100#	GBE0_LINK_MID#
P22	GBE_LINK1000#	GBE0_LINK1000#	GBE0_LINK1000#	GBE0_LINK_MAX#
P23	GBE_MDI2-	GBE0_MDI2-	GBE0_MDI2-	GBE0_MDI2-
P24	GBE_MDI2+	GBE0_MDI2+	GBE0_MDI2+	GBE0_MDI2+
P25	GBE_LINK_ACT#	GBE0_LINK_ACT#	GBE0_LINK_ACT#	GBE0_LINK_ACT#
P26	GBE_MDI1-	GBE0_MDI1-	GBE0_MDI1-	GBE0_MDI1-
P27	GBE_MDI1+	GBE0_MDI1+	GBE0_MDI1+	GBE0_MDI1+
P28	GBE_CTREF	GBE0_CTREF	GBE0_CTREF	GBE0_CTREF
P29	GBE_MDI0-	GBE0_MDI0-	GBE0_MDI0-	GBE0_MDI0-
P30	GBE_MDI0+	GBE0_MDI0+	GBE0_MDI0+	GBE0_MDI0+
P31	SPI0_CS1#	SPI0_CS1#	SPI0_CS1#	SPI0_CS1#
P32	GND	GND	GND	GND
P33	SDIO_WP	SDIO_WP	SDIO_WP	SDIO_WP
P34	SDIO_CMD	SDIO_CMD	SDIO_CMD	SDIO_CMD
P35	SDIO_CD#	SDIO_CD#	SDIO_CD#	SDIO_CD#
P36	SDIO_CK	SDIO_CK	SDIO_CK	SDIO_CK
P37	SDIO_PWR_EN	SDIO_PWR_EN	SDIO_PWR_EN	SDIO_PWR_EN
P38	GND	GND	GND	GND

Pin	SMARC 1.1	SMARC 2.0	SMARC 2.1	SMARC 2.2
P39	SDIO_D0	SDIO_D0	SDIO_D0	SDIO_D0
P40	SDIO_D1	SDIO_D1	SDIO_D1	SDIO_D1
P41	SDIO_D2	SDIO_D2	SDIO_D2	SDIO_D2
P42	SDIO_D3	SDIO_D3	SDIO_D3	SDIO_D3
P43	SPI0_CS0#	SPI0_CS0#	SPI0_CS0#	SPI0_CS0#
P44	SPI0_CK	SPI0_CK	SPI0_CK	SPI0_CK
P45	SPI0_DIN	SPI0_DIN	SPI0_DIN	SPI0_DIN
P46	SPI0_DO	SPI0_DO	SPI0_DO	SPI0_DO
P47	GND	GND	GND	GND
P48	SATA_TX+	SATA_TX+	SATA_TX+	SATA_TX+
P49	SATA_TX-	SATA_TX-	SATA_TX-	SATA_TX-
P50	GND	GND	GND	GND
P51	SATA_RX+	SATA_RX+	SATA_RX+	SATA_RX+
P52	SATA_RX-	SATA_RX-	SATA_RX-	SATA_RX-
P53	GND	GND	GND	GND
P54	SPI1_CS0#	SPI1_CS0# **/ ESPI_CS0#**	SPI1_CS0# / ESPI_CS0# **/ QSPI_CS0#**	SPI1_CS0# / ESPI_CS0# **/** QSPI_CS0#
P55	SPI1_CS1#	SPI1_CS1# **/ ESPI_CS1#**	SPI1_CS1# / ESPI_CS1# **/ QSPI_CS1#**	SPI1_CS1# / ESPI_CS1# **/** QSPI_CS1#
P56	SPI1_CK	SPI1_CK **/ ESPI_CK**	SPI1_CK / ESPI_CK **/ QSPI_CK**	SPI1_CK / ESPI_CK **/** QSPI_CK
P57	SPI1_DIN	SPI1_DIN **/ ESPI_IO_1**	SPI1_DIN / ESPI_IO_1 **/ QSPI_IO_1**	SPI1_DIN / ESPI_IO_1 **/** QSPI_IO_1
P58	SPI1_DO	SPI1_DO **/ ESPI_IO_0**	SPI1_DO / ESPI_IO_0 **/ QSPI_IO_0**	SPI1_DO / ESPI_IO_0 **/** QSPI_IO_0
P59	GND	GND	GND	GND
P60	USB0+	USB0+	USB0+	USB0+
P61	USB0-	USB0-	USB0-	USB0-
P62	USB0_EN_OC#	USB0_EN_OC#	USB0_EN_OC#	USB0_EN_OC#
P63	USB0_VBUS_DET	USB0_VBUS_DET	USB0_VBUS_DET	USB0_VBUS_DET
P64	USB0_OTG_ID	USB0_OTG_ID	USB0_OTG_ID	USB0_OTG_ID
P65	USB1+	USB1+	USB1+	USB1+
P66	USB1-	USB1-	USB1-	USB1-
P67	USB1_EN_OC#	USB1_EN_OC#	USB1_EN_OC#	USB1_EN_OC#
P68	GND	GND	GND	GND
P69	USB2+	USB2+	USB2+	USB2+
P70	USB2-	USB2-	USB2-	USB2-
P71	USB2_EN_OC#	USB2_EN_OC#	USB2_EN_OC#	USB2_EN_OC#
P72	~~PCIE_C_PRSNT#~~	**RSVD**	RSVD	RSVD
P73	~~PCIE_B_PRSNT#~~	**RSVD**	RSVD	RSVD
P74	~~PCIE_A_PRSNT#~~	**USB3_EN_OC#**	USB3_EN_OC#	USB3_EN_OC#
P75	PCIE_A_RST#	PCIE_A_RST#	PCIE_A_RST#	PCIE_A_RST#
P76	~~PCIE_C_CKREQ#~~	**USB4_EN_OC#**	USB4_EN_OC#	USB4_EN_OC#
P77	~~PCIE_B_CKREQ#~~	**RSVD**	**PCIE_B_CKREQ#**	PCIE_B_CKREQ#
P78	~~PCIE_A_CKREQ#~~	**RSVD**	**PCIE_A_CKREQ#**	PCIE_A_CKREQ#

Pin	SMARC 1.1	SMARC 2.0	SMARC 2.1	SMARC 2.2
P79	GND	GND	GND	GND
P80	PCIE_C_REFCK+	PCIE_C_REFCK+	PCIE_C_REFCK+	PCIE_C_REFCK+
P81	PCIE_C_REFCK-	PCIE_C_REFCK-	PCIE_C_REFCK-	PCIE_C_REFCK-
P82	GND	GND	GND	GND
P83	PCIE_A_REFCK+	PCIE_A_REFCK+	PCIE_A_REFCK+	PCIE_A_REFCK+
P84	PCIE_A_REFCK-	PCIE_A_REFCK-	PCIE_A_REFCK-	PCIE_A_REFCK-
P85	GND	GND	GND	GND
P86	PCIE_A_RX+	PCIE_A_RX+	PCIE_A_RX+	PCIE_A_RX+
P87	PCIE_A_RX-	PCIE_A_RX-	PCIE_A_RX-	PCIE_A_RX-
P88	GND	GND	GND	GND
P89	PCIE_A_TX+	PCIE_A_TX+	PCIE_A_TX+	PCIE_A_TX+
P90	PCIE_A_TX-	PCIE_A_TX-	PCIE_A_TX-	PCIE_A_TX-
P91	GND	GND	GND	GND
P92	HDMI_D2+	HDMI_D2+ **/ DP1_LANE0+**	HDMI_D2+ / DP1_LANE0+	HDMI_D2+ / DP1_LANE0+
P93	HDMI_D2-	HDMI_D2- **/ DP1_LANE0-**	HDMI_D2- / DP1_LANE0-	HDMI_D2- / DP1_LANE0-
P94	GND	GND	GND	GND
P95	HDMI_D1+	HDMI_D1+ **/ DP1_LANE1+**	HDMI_D1+ / DP1_LANE1+	HDMI_D1+ / DP1_LANE1+
P96	HDMI_D1-	HDMI_D1- **/ DP1_LANE1-**	HDMI_D1- / DP1_LANE1-	HDMI_D1- / DP1_LANE1-
P97	GND	GND	GND	GND
P98	HDMI_D0+	HDMI_D0+ **/ DP1_LANE2+**	HDMI_D0+ / DP1_LANE2+	HDMI_D0+ / DP1_LANE2+
P99	HDMI_D0-	HDMI_D0- **/ DP1_LANE2-**	HDMI_D0- / DP1_LANE2-	HDMI_D0- / DP1_LANE2-
P100	GND	GND	GND	GND
P101	HDMI_CK+	HDMI_CK+ **/ DP1_LANE3+**	HDMI_CK+ / DP1_LANE3+	HDMI_CK+ / DP1_LANE3+
P102	HDMI_CK-	HDMI_CK- **/ DP1_LANE3-**	HDMI_CK- / DP1_LANE3-	HDMI_CK- / DP1_LANE3-
P103	GND	GND	GND	GND
P104	HDMI_HPD	HDMI_HPD **/ DP1_HPD**	HDMI_HPD / DP1_HPD	HDMI_HPD / DP1_HPD
P105	HDMI_CTRL_CK	HDMI_CTRL_CK **/ DP1_AUX+**	HDMI_CTRL_CK / DP1_AUX+	HDMI_CTRL_CK / DP1_AUX+
P106	HDMI_CTRL_DAT	HDMI_CTRL_DAT **/ DP1_AUX-**	HDMI_CTRL_DAT / DP1_AUX-	HDMI_CTRL_DAT / DP1_AUX-
P107	~~**HDMI_CEC**~~	**DP1_AUX_SEL**	DP1_AUX_SEL	DP1_AUX_SEL
P108	GPIO0 / CAM0_PWR#	GPIO0 / CAM0_PWR#	GPIO0 / CAM0_PWR#	GPIO0 / CAM0_PWR#
P109	GPIO1 / CAM1_PWR#	GPIO1 / CAM1_PWR#	GPIO1 / CAM1_PWR#	GPIO1 / CAM1_PWR#
P110	GPIO2 / CAM0_RST#	GPIO2 / CAM0_RST#	GPIO2 / CAM0_RST#	GPIO2 / CAM0_RST#
P111	GPIO3 / CAM1_RST#	GPIO3 / CAM1_RST#	GPIO3 / CAM1_RST#	GPIO3 / CAM1_RST#
P112	GPIO4 / HDA_RST#	GPIO4 / HDA_RST#	GPIO4 / HDA_RST#	GPIO4 / HDA_RST#
P113	GPIO5 / PWM_OUT	GPIO5 / PWM_OUT	GPIO5 / PWM_OUT	GPIO5 / PWM_OUT
P114	GPIO6 / TACHIN	GPIO6 / TACHIN	GPIO6 / TACHIN	GPIO6 / TACHIN
P115	GPIO7 ~~**/ PCAM_FLD**~~	GPIO7	GPIO7	GPIO7
P116	GPIO8 ~~**/ CAN0_ERR#**~~	GPIO8	GPIO8	GPIO8
P117	GPIO9 ~~**/ CAN1_ERR#**~~	GPIO9	GPIO9	GPIO9
P118	GPIO10	GPIO10	GPIO10	GPIO10

Pin	SMARC 1.1	SMARC 2.0	SMARC 2.1	SMARC 2.2
P119	GPIO11	GPIO11	GPIO11	GPIO11
P120	GND	GND	GND	GND
P121	I2C_PM_CK	I2C_PM_CK	I2C_PM_CK	I2C_PM_CK
P122	I2C_PM_DAT	I2C_PM_DAT	I2C_PM_DAT	I2C_PM_DAT
P123	BOOT_SEL0#	BOOT_SEL0#	BOOT_SEL0#	BOOT_SEL0#
P124	BOOT_SEL1#	BOOT_SEL1#	BOOT_SEL1#	BOOT_SEL1#
P125	BOOT_SEL2#	BOOT_SEL2#	BOOT_SEL2#	BOOT_SEL2#
P126	RESET_OUT#	RESET_OUT#	RESET_OUT#	RESET_OUT#
P127	RESET_IN#	RESET_IN#	RESET_IN#	RESET_IN#
P128	POWER_BTN#	POWER_BTN#	POWER_BTN#	POWER_BTN#
P129	SER0_TX	SER0_TX	SER0_TX	SER0_TX
P130	SER0_RX	SER0_RX	SER0_RX	SER0_RX
P131	SER0_RTS#	SER0_RTS#	SER0_RTS#	SER0_RTS#
P132	SER0_CTS#	SER0_CTS#	SER0_CTS#	SER0_CTS#
P133	GND	GND	GND	GND
P134	SER1_TX	SER1_TX	SER1_TX	SER1_TX
P135	SER1_RX	SER1_RX	SER1_RX	SER1_RX
P136	SER2_TX	SER2_TX	SER2_TX	SER2_TX
P137	SER2_RX	SER2_RX	SER2_RX	SER2_RX
P138	SER2_RTS#	SER2_RTS#	SER2_RTS#	SER2_RTS#
P139	SER2_CTS#	SER2_CTS#	SER2_CTS#	SER2_CTS#
P140	SER3_TX	SER3_TX	SER3_TX	SER3_TX
P141	SER3_RX	SER3_RX	SER3_RX	SER3_RX
P142	GND	GND	GND	GND
P143	CAN0_TX	CAN0_TX	CAN0_TX	CAN0_TX
P144	CAN0_RX	CAN0_RX	CAN0_RX	CAN0_RX
P145	CAN1_TX	CAN1_TX	CAN1_TX	CAN1_TX
P146	CAN1_RX	CAN1_RX	CAN1_RX	CAN1_RX
P147	VDD_IN	VDD_IN	VDD_IN	VDD_IN
P148	VDD_IN	VDD_IN	VDD_IN	VDD_IN
P149	VDD_IN	VDD_IN	VDD_IN	VDD_IN
P150	VDD_IN	VDD_IN	VDD_IN	VDD_IN
P151	VDD_IN	VDD_IN	VDD_IN	VDD_IN
P152	VDD_IN	VDD_IN	VDD_IN	VDD_IN
P153	VDD_IN	VDD_IN	VDD_IN	VDD_IN
P154	VDD_IN	VDD_IN	VDD_IN	VDD_IN
P155	VDD_IN	VDD_IN	VDD_IN	VDD_IN
P156	VDD_IN	VDD_IN	VDD_IN	VDD_IN

Pin	SMARC 1.1	SMARC 2.0	SMARC 2.1	SMARC 2.2
S1	~~PCAM_VSYNC~~	CSI1_TX+ / I2C_CAM1_CK	CSI1_TX+ / I2C_CAM1_CK	CSI1_TX+ / I2C_CAM1_CK
S2	~~PCAM_HSYNC~~	CSI1_TX- / I2C_CAM1_DAT	CSI1_TX- / I2C_CAM1_DAT	CSI1_TX- / I2C_CAM1_DAT
S3	GND	GND	GND	GND
S4	~~PCAM_PXL_CK0~~	RSVD	RSVD	RSVD
S5	I2C_CAM_CK	I2C_CAM0_CK / CSI0_TX+	I2C_CAM0_CK / CSI0_TX+	I2C_CAM0_CK / CSI0_TX+
S6	CAM_MCK	CAM_MCK	CAM_MCK	CAM_MCK
S7	I2C_CAM_DAT	I2C_CAM0_DAT / CSI0_TX-	I2C_CAM0_DAT / CSI0_TX-	I2C_CAM0_DAT / CSI0_TX-
S8	CSI0_CK+ ~~/ PCAM_D10~~	CSI0_CK+	CSI0_CK+	CSI0_CK+
S9	CSI0_CK- ~~/ PCAM_D11~~	CSI0_CK-	CSI0_CK-	CSI0_CK-
S10	GND	GND	GND	GND
S11	CSI0_D0+ ~~/ PCAM_D12~~	CSI0_RX0+	CSI0_RX0+	CSI0_RX0+
S12	CSI0_D0- ~~/ PCAM_D13~~	CSI0_RX0-	CSI0_RX0-	CSI0_RX0-
S13	GND	GND	GND	GND
S14	CSI0_D1+ ~~/ PCAM_D14~~	CSI0_RX1+	CSI0_RX1+	CSI0_RX1+
S15	CSI0_D1- ~~/ PCAM_D15~~	CSI0_RX1-	CSI0_RX1-	CSI0_RX1-
S16	GND	GND	GND	GND
S17	~~AFB0_OUT~~	GBE1_MDI0+	GBE1_MDI0+	GBE1_MDI0+
S18	~~AFB1_OUT~~	GBE1_MDI0-	GBE1_MDI0-	GBE1_MDI0-
S19	~~AFB2_OUT~~	GBE1_LINK100#	GBE1_LINK100#	GBE1_LINK_MID#
S20	~~AFB3_IN~~	GBE1_MDI1+	GBE1_MDI1+	GBE1_MDI1+
S21	~~AFB4_IN~~	GBE1_MDI1-	GBE1_MDI1-	GBE1_MDI1-
S22	~~AFB5_IN~~	GBE1_LINK1000#	GBE1_LINK1000#	GBE1_LINK_MAX#
S23	~~AFB6_PTIO~~	GBE1_MDI2+	GBE1_MDI2+	GBE1_MDI2+
S24	~~AFB7_PTIO~~	GBE1_MDI2-	GBE1_MDI2-	GBE1_MDI2-
S25	GND	GND	GND	GND
S26	~~SDMMC_D0~~	GBE1_MDI3+	GBE1_MDI3+	GBE1_MDI3+
S27	~~SDMMC_D1~~	GBE1_MDI3-	GBE1_MDI3-	GBE1_MDI3-
S28	~~SDMMC_D2~~	GBE1_CTREF	GBE1_CTREF	GBE1_CTREF
S29	~~SDMMC_D3~~	PCIE_D_TX+	PCIE_D_TX+ / SERDES_0_TX+	PCIE_D_TX+ / SERDES_0_TX+
S30	~~SDMMC_D4~~	PCIE_D_TX-	PCIE_D_TX- / SERDES_0_TX-	PCIE_D_TX- / SERDES_0_TX-
S31	~~SDMMC_D5~~	GBE1_LINK_ACT#	GBE1_LINK_ACT#	GBE1_LINK_ACT#
S32	~~SDMMC_D6~~	PCIE_D_RX+	PCIE_D_RX+ / SERDES_0_RX+	PCIE_D_RX+ / SERDES_0_RX+
S33	~~SDMMC_D7~~	PCIE_D_RX-	PCIE_D_RX- / SERDES_0_RX-	PCIE_D_RX- / SERDES_0_RX-
S34	GND	GND	GND	GND
S35	~~SDMMC_CK~~	USB4+	USB4+	USB4+
S36	~~SDMMC_CMD~~	USB4-	USB4-	USB4-
S37	~~SDMMC_RST#~~	USB3_VBUS_DET	USB3_VBUS_DET	USB3_VBUS_DET
S38	AUDIO_MCK	AUDIO_MCK	AUDIO_MCK	AUDIO_MCK
S39	I2S0_LRCK	I2S0_LRCK	I2S0_LRCK	I2S0_LRCK
S40	I2S0_SDOUT	I2S0_SDOUT	I2S0_SDOUT	I2S0_SDOUT

Pin	SMARC 1.1	SMARC 2.0	SMARC 2.1	SMARC 2.2
S41	I2S0_SDIN	I2S0_SDIN	I2S0_SDIN	I2S0_SDIN
S42	I2S0_CK	I2S0_CK	I2S0_CK	I2S0_CK
S43	~~I2S1_LRCK~~	ESPI_ALERT0#	ESPI_ALERT0#	ESPI_ALERT0#
S44	~~I2S1_SDOUT~~	ESPI_ALERT1#	ESPI_ALERT1#	ESPI_ALERT1#
S45	~~I2S1_SDIN~~	RSVD	MDIO_CLK	MDIO_CLK
S46	~~I2S1_CK~~	RSVD	MDIO_DAT	MDIO_DAT
S47	GND	GND	GND	GND
S48	I2C_GP_CK	I2C_GP_CK	I2C_GP_CK	I2C_GP_CK
S49	I2C_GP_DAT	I2C_GP_DAT	I2C_GP_DAT	I2C_GP_DAT
S50	I2S2_LRCK	I2S2_LRCK / HDA_SYNC	I2S2_LRCK / HDA_SYNC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1
S51	I2S2_SDOUT	I2S2_SDOUT / HDA_SDO	I2S2_SDOUT / HDA_SDO	I2S2_SDOUT / HDA_SDO / SNDW_DAT1
S52	I2S2_SDIN	I2S2_SDIN / HDA_SDI	I2S2_SDIN / HDA_SDI	I2S2_SDIN / HDA_SDI / SNDW_DAT0
S53	I2S2_CK	I2S2_CK / HDA_CK	I2S2_CK / HDA_CK	I2S2_CK / HDA_CK / SNDW_CLK0
S54	SATA_ACT#	SATA_ACT#	SATA_ACT#	SATA_ACT#
S55	~~AFB8_PTIO~~	USB5_EN_OC#	USB5_EN_OC#	USB5_EN_OC#
S56	~~AFB9_PTIO~~	ESPI_IO_2	ESPI_IO_2 / QSPI_IO_2	ESPI_IO_2 / QSPI_IO_2
S57	~~PCAM_ON_CSI0#~~	ESPI_IO_3	ESPI_IO_3 / QSPI_IO_3	ESPI_IO_3 / QSPI_IO_3
S58	~~PCAM_ON_CSI1#~~	ESPI_RESET#	ESPI_RESET#	ESPI_RESET#
S59	~~SPDIF_OUT~~	USB5+	USB5+	USB5+
S60	~~SPDIF_IN~~	USB5-	USB5-	USB5-
S61	GND	GND	GND	GND
S62	~~AFB_DIFF0+~~	USB3_SSTX+	USB3_SSTX+	USB3_SSTX+
S63	~~AFB_DIFF0-~~	USB3_SSTX-	USB3_SSTX-	USB3_SSTX-
S64	GND	GND	GND	GND
S65	~~AFB_DIFF1+~~	USB3_SSRX+	USB3_SSRX+	USB3_SSRX+
S66	~~AFB_DIFF1-~~	USB3_SSRX-	USB3_SSRX-	USB3_SSRX-
S67	GND	GND	GND	GND
S68	~~AFB_DIFF2+~~	USB3+	USB3+	USB3+
S69	~~AFB_DIFF2-~~	USB3-	USB3-	USB3-
S70	GND	GND	GND	GND
S71	~~AFB_DIFF3+~~	USB2_SSTX+	USB2_SSTX+	USB2_SSTX+
S72	~~AFB_DIFF3-~~	USB2_SSTX-	USB2_SSTX-	USB2_SSTX-
S73	GND	GND	GND	GND
S74	~~AFB_DIFF4+~~	USB2_SSRX+	USB2_SSRX+	USB2_SSRX+
S75	~~AFB_DIFF4-~~	USB2_SSRX-	USB2_SSRX-	USB2_SSRX-
S76	PCIE_B_RST#	PCIE_B_RST#	PCIE_B_RST#	PCIE_B_RST#
S77	PCIE_C_RST#	PCIE_C_RST#	PCIE_C_RST#	PCIE_C_RST#
S78	PCIE_C_RX+	PCIE_C_RX+	PCIE_C_RX+ / SERDES_1_RX+	PCIE_C_RX+ / SERDES_1_RX+
S79	PCIE_C_RX-	PCIE_C_RX-	PCIE_C_RX- / SERDES_1_RX-	PCIE_C_RX- / SERDES_1_RX-
S80	GND	GND	GND	GND

Pin	SMARC 1.1	SMARC 2.0	SMARC 2.1	SMARC 2.2
S81	PCIE_C_TX+	PCIE_C_TX+	PCIE_C_TX+ / SERDES_1_TX+	PCIE_C_TX+ / SERDES_1_TX+
S82	PCIE_C_TX-	PCIE_C_TX-	PCIE_C_TX- / SERDES_1_TX-	PCIE_C_TX- / SERDES_1_TX-
S83	GND	GND	GND	GND
S84	PCIE_B_REFCK+	PCIE_B_REFCK+	PCIE_B_REFCK+	PCIE_B_REFCK+
S85	PCIE_B_REFCK-	PCIE_B_REFCK-	PCIE_B_REFCK-	PCIE_B_REFCK-
S86	GND	GND	GND	GND
S87	PCIE_B_RX+	PCIE_B_RX+	PCIE_B_RX+	PCIE_B_RX+
S88	PCIE_B_RX-	PCIE_B_RX-	PCIE_B_RX-	PCIE_B_RX-
S89	GND	GND	GND	GND
S90	PCIE_B_TX+	PCIE_B_TX+	PCIE_B_TX+	PCIE_B_TX+
S91	PCIE_B_TX-	PCIE_B_TX-	PCIE_B_TX-	PCIE_B_TX-
S92	GND	GND	GND	GND
S93	~~LCD_D0~~	DP0_LANE0+	DP0_LANE0+	DP0_LANE0+
S94	~~LCD_D1~~	DP0_LANE0-	DP0_LANE0-	DP0_LANE0-
S95	~~LCD_D2~~	DP0_AUX_SEL	DP0_AUX_SEL	DP0_AUX_SEL
S96	~~LCD_D3~~	DP0_LANE1+	DP0_LANE1+	DP0_LANE1+
S97	~~LCD_D4~~	DP0_LANE1-	DP0_LANE1-	DP0_LANE1-
S98	~~LCD_D5~~	DP0_HPD	DP0_HPD	DP0_HPD
S99	~~LCD_D6~~	DP0_LANE2+	DP0_LANE2+	DP0_LANE2+
S100	~~LCD_D7~~	DP0_LANE2-	DP0_LANE2-	DP0_LANE2-
S101	GND	GND	GND	GND
S102	~~LCD_D8~~	DP0_LANE3+	DP0_LANE3+	DP0_LANE3+
S103	~~LCD_D9~~	DP0_LANE3-	DP0_LANE3-	DP0_LANE3-
S104	~~LCD_D10~~	USB3_OTG_ID	USB3_OTG_ID	USB3_OTG_ID
S105	~~LCD_D11~~	DP0_AUX+	DP0_AUX+	DP0_AUX+
S106	~~LCD_D12~~	DP0_AUX-	DP0_AUX-	DP0_AUX-
S107	~~LCD_D13~~	LCD1_BKLT_EN	LCD1_BKLT_EN	LCD1_BKLT_EN
S108	~~LCD_D14~~	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+
S109	~~LCD_D15~~	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-
S110	GND	GND	GND	GND
S111	~~LCD_D16~~	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+
S112	~~LCD_D17~~	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_0- / eDP1_TX0- / DSI1_D0-
S113	~~LCD_D18~~	eDP1_HPD	eDP1_HPD / DSI1_TE	eDP1_HPD / DSI1_TE
S114	~~LCD_D19~~	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+
S115	~~LCD_D20~~	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_1- / eDP1_TX1- / DSI1_D1-
S116	~~LCD_D21~~	LCD1_VDD_EN	LCD1_VDD_EN	LCD1_VDD_EN
S117	~~LCD_D22~~	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+
S118	~~LCD_D23~~	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_2- / eDP1_TX2- / DSI1_D2-
S119	GND	GND	GND	GND

Pin	SMARC 1.1	SMARC 2.0	SMARC 2.1	SMARC 2.2
S120	~~LCD_DE~~	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+
S121	~~LCD_VS~~	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_3- / eDP1_TX3- / DSI1_D3-
S122	~~LCD_HS~~	LCD1_BKLT_PWM	LCD1_BKLT_PWM	LCD1_BKLT_PWM
S123	~~LCD_PCK~~	RSVD	GPIO13	GPIO13
S124	GND	GND	GND	GND
S125	LVDS0+	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+
S126	LVDS0-	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0_0- / eDP0_TX0- / DSI0_D0-
S127	LCD_BKLT_EN	LCD0_BKLT_EN	LCD0_BKLT_EN	LCD0_BKLT_EN
S128	LVDS1+	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+
S129	LVDS1-	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0_1- / eDP0_TX1- / DSI0_D1-
S130	GND	GND	GND	GND
S131	LVDS2+	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+
S132	LVDS2-	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0_2- / eDP0_TX2- / DSI0_D2-
S133	LCD_VDD_EN	LCD0_VDD_EN	LCD0_VDD_EN	LCD0_VDD_EN
S134	LVDS_CK+	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+
S135	LVDS_CK-	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-
S136	GND	GND	GND	GND
S137	LVDS3+	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+
S138	LVDS3-	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0_3- / eDP0_TX3- / DSI0_D3-
S139	I2C_LCD_CK	I2C_LCD_CK	I2C_LCD_CK	I2C_LCD_CK
S140	I2C_LCD_DAT	I2C_LCD_DAT	I2C_LCD_DAT	I2C_LCD_DAT
S141	LCD_BKLT_PWM	LCD0_BKLT_PWM	LCD0_BKLT_PWM	LCD0_BKLT_PWM
S142	RSVD	RSVD	GPIO12	GPIO12
S143	GND	GND	GND	GND
S144	~~RSVD /~~ EDP_HPD	eDP0_HPD	eDP0_HPD / DSI0_TE	eDP0_HPD / DSI0_TE
S145	WDT_TIME_OUT#	WDT_TIME_OUT#	WDT_TIME_OUT#	WDT_TIME_OUT#
S146	PCIE_WAKE#	PCIE_WAKE#	PCIE_WAKE#	PCIE_WAKE#
S147	VDD_RTC	VDD_RTC	VDD_RTC	VDD_RTC
S148	LID#	LID#	LID#	LID#
S149	SLEEP#	SLEEP#	SLEEP#	SLEEP#
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	VIN_PWR_BAD#	VIN_PWR_BAD#
S151	CHARGING#	CHARGING#	CHARGING#	CHARGING#
S152	CHARGER_PRSNT#	CHARGER_PRSNT#	CHARGER_PRSNT#	CHARGER_PRSNT#
S153	CARRIER_STBY#	CARRIER_STBY#	CARRIER_STBY#	CARRIER_STBY#
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	CARRIER_PWR_ON	CARRIER_PWR_ON
S155	FORCE_RECOV#	FORCE_RECOV#	FORCE_RECOV#	FORCE_RECOV#
S156	BATLOW#	BATLOW#	BATLOW#	BATLOW#
S157	TEST#	TEST#	TEST#	TEST#
S158	GND	GND	GND	GND

9.6 Signal Name Index

Audio

AUDIO_MCK 39, 40, 70, 103
HDA_CK 40, 41, 70, 104
HDA_RST# 40, 41, 59, 60, 61, 72, 101
HDA_SDI 40, 41, 70, 104
HDA_SDO 40, 41, 70, 104
HDA_SYNC 40, 41, 70, 104
I2S0_CK 39, 70, 104
I2S0_LRCK 39, 70, 103
I2S0_SDIN 39, 70, 104
I2S0_SDOUT 39, 70, 103
I2S2_CK 40, 41, 70, 104
I2S2_LRCK 40, 41, 70, 104
I2S2_SDIN 40, 41, 70, 104
I2S2_SDOUT 40, 41, 70, 104
SNDW_CLK0 ..... 41, 70, 104
SNDW_CLK1 ..... 41, 70, 104
SNDW_DAT0 ..... 41, 70, 104
SNDW_DAT1 ..... 41, 70, 104

Camera

CAM_MCK 30, 32, 69, 103
CAM0_PWR# 29, 59, 60, 61, 72, 101
CAM0_RST# 29, 59, 60, 61, 72, 101
CAM1_PWR# 30, 59, 60, 61, 72, 101
CAM1_RST# 30, 59, 60, 61, 72, 101
CAM2_MCK 31
CAM2_PWR# 31
CAM2_RST# 31
CAM2_VCC 31
CAM3_MCK 32
CAM3_PWR# 32
CAM3_RST# 32
CAM3_VCC 32
CSI0_CK- 29, 69, 103
CSI0_CK+ 29, 69, 103
CSI0_RX0- 29, 69, 103
CSI0_RX0+ 29, 69, 103
CSI0_RX1- 29, 69, 103
CSI0_RX1+ 29, 69, 103
CSI0_TX- 29, 69, 103
CSI0_TX+ 29, 69, 103
CSI1_CK- 30, 69, 99
CSI1_CK+ 30, 69, 99
CSI1_RX0- 29, 69, 99
CSI1_RX0+ 29, 69, 99
CSI1_RX1- 29, 69, 99
CSI1_RX1+ 29, 69, 99
CSI1_RX2- 29, 69, 99
CSI1_RX2+ 29, 69, 99
CSI1_RX3- 29, 31, 69, 99
CSI1_RX3+ 29, 69, 99
CSI1_TX- 30, 31, 32, 69, 103
CSI1_TX+ 30, 31, 32, 69, 103
CSI2_CK- 31
CSI2_CK+ 31
CSI2_RX0- 31
CSI2_RX0+ 31
CSI2_RX1- 31
CSI2_RX1+ 31
CSI2_RX2- 31
CSI2_RX2+ 31
CSI2_RX3- 31
CSI2_RX3+ 31
CSI2_TX- 31
CSI2_TX+ 31
CSI3_CK- 32
CSI3_CK+ 32
CSI3_RX0- 32
CSI3_RX0+ 32
CSI3_RX1- 32
CSI3_RX1+ 32
CSI3_RX2- 32
CSI3_RX2+ 32
CSI3_RX3- 32
CSI3_RX3+ 32
CSI3_TX- 32
CSI3_TX+ 32
I2C_CAM0_CK 29, 69, 103
I2C_CAM0_DAT 29, 69, 103
I2C_CAM1_CK 30, 31, 32, 69, 103
I2C_CAM1_DAT 30, 31, 32, 69, 103
I2C_CAM2_CK 31
I2C_CAM2_DAT 31
I2C_CAM3_CK 32
I2C_CAM3_DAT 32

CAN

CAN0_RX 44, 73, 102
CAN0_TX 44, 73, 102
CAN1_RX 44, 73, 102
CAN1_TX 44, 73, 102

Display

DP0_AUX- 21, 24, 28, 72, 73, 105, 106
DP0_AUX_SEL 28, 71, 105
DP0_AUX+ 28, 72, 73, 105, 106
DP0_HPD 28, 72, 105
DP0_LANE0- 28, 71, 105

DP0_LANE0+ 28, 71, 105
DP0_LANE1- 28, 72, 105
DP0_LANE1+ 28, 71, 105
DP0_LANE2- 28, 72, 105
DP0_LANE2+ 28, 72, 105
DP0_LANE3- 28, 72, 105
DP0_LANE3+ 28, 72, 105
DP1_AUX- 21, 24, 26, 27, 72, 101, 105
DP1_AUX_SEL 26, 72, 101
DP1_AUX+ 26, 27, 72, 101, 105
DP1_HPD 26, 27, 72, 101
DP1_LANE0- 26, 27, 71, 101
DP1_LANE0+ 26, 27, 71, 101
DP1_LANE1- 26, 27, 72, 101
DP1_LANE1+ 26, 27, 71, 101
DP1_LANE2- 26, 27, 72, 101
DP1_LANE2+ 26, 27, 72, 101
DP1_LANE3- 26, 27, 72, 101
DP1_LANE3+ 26, 27, 72, 101
DSI0_CLK- 23, 24, 73, 106
DSI0_CLK+ 23, 24, 73, 106
DSI0_D0- 23, 24, 72, 106
DSI0_D0+ 23, 24, 72, 106
DSI0_D1- 23, 24, 72, 106
DSI0_D1+ 23, 24, 72, 106
DSI0_D2- 23, 24, 72, 106
DSI0_D2+ 23, 24, 72, 106
DSI0_D3- 23, 24, 73, 106
DSI0_D3+ 23, 24, 73, 106
DSI0_TE 23, 24, 73, 106
DSI1_CLK- 23, 24, 72, 105
DSI1_CLK+ 23, 24, 72, 105
DSI1_D0- 23, 24, 72, 105
DSI1_D0+ 23, 24, 72, 105
DSI1_D1- 23, 24, 72, 105
DSI1_D1+ 23, 24, 72, 105
DSI1_D2- 23, 24, 72, 105
DSI1_D2+ 23, 24, 72, 105
DSI1_D3- 23, 24, 72, 106
DSI1_D3+ 23, 24, 72, 106
DSI1_TE 23, 24, 72, 105
eDP0_AUX- 21, 24, 73, 106
eDP0_AUX+ 21, 24, 73, 106
eDP0_HPD 21, 24, 73, 106
eDP0_TX0- 21, 24, 72, 106
eDP0_TX0+ 21, 24, 72, 106
eDP0_TX1- 21, 24, 72, 106
eDP0_TX1+ 21, 24, 72, 106
eDP0_TX2- 21, 24, 72, 106
eDP0_TX2+ 21, 24, 72, 106
eDP0_TX3- 21, 24, 73, 106
eDP0_TX3+ 21, 24, 73, 106
eDP1_AUX- 21, 24, 72, 105
eDP1_AUX+ 21, 24, 72, 105
eDP1_HPD 22, 24, 72, 105
eDP1_TX0- 21, 24, 72, 105
eDP1_TX0+ 21, 24, 72, 105
eDP1_TX1- 21, 24, 72, 105
eDP1_TX1+ 21, 24, 72, 105
eDP1_TX2- 21, 24, 72, 105
eDP1_TX2+ 21, 24, 72, 105
eDP1_TX3- 21, 24, 72, 106
eDP1_TX3+ 21, 24, 72, 106
HDMI_CK- 25, 27, 72, 101
HDMI_CK+ 25, 27, 72, 101
HDMI_CTRL_CK 25, 26, 27, 72, 101
HDMI_CTRL_DAT 25, 26, 27, 72, 101
HDMI_D0- 25, 27, 72, 101
HDMI_D0+ 25, 27, 72, 101
HDMI_D1- 25, 27, 72, 101
HDMI_D1+ 25, 27, 71, 101
HDMI_D2- 25, 27, 71, 101
HDMI_D2+ 25, 27, 71, 101
HDMI_HPD 25, 27, 72, 101
LCD0_BKLT_EN 20, 21, 23, 24, 72, 106
LCD0_BKLT_PWM 20, 21, 23, 24, 73, 106
LCD0_VDD_EN 19, 21, 23, 24, 73, 106
LCD1_BKLT_EN 20, 21, 23, 24, 72, 105
LCD1_BKLT_PWM 20, 22, 23, 24, 72, 106
LCD1_VDD_EN 20, 21, 23, 24, 72, 105
LVDS0_0- 19, 24, 72, 106
LVDS0_0+ 19, 24, 72, 106
LVDS0_1- 19, 72, 106
LVDS0_1+ 19, 24, 72, 106
LVDS0_2- 19, 24, 72, 106
LVDS0_2+ 19, 24, 72, 106
LVDS0_3- 19, 24, 73, 106
LVDS0_3+ 19, 24, 73, 106
LVDS0_CK- 19, 24, 73, 106
LVDS0_CK+ 19, 24, 73, 106
LVDS1_0- 20, 24, 72, 105
LVDS1_0+ 20, 24, 72, 105
LVDS1_1- 20, 72, 105
LVDS1_1+ 20, 24, 72, 105
LVDS1_2- 20, 24, 72, 105
LVDS1_2+ 20, 24, 72, 105
LVDS1_3- 20, 24, 72, 106
LVDS1_3+ 20, 24, 72, 106
LVDS1_CK- 20, 24, 72, 105
LVDS1_CK+ 20, 24, 72, 105

ESPI

ESPI_ALERT0# 38, 70, 104
ESPI_ALERT1# 38, 70, 104
ESPI_CK 38, 70, 100
ESPI_CS0# 38, 70, 100
ESPI_CS1# 38, 70, 100
ESPI_IO_0 38, 70, 100
ESPI_IO_1 38, 70, 100
ESPI_IO_2 38, 70, 104
ESPI_IO_3 38, 70, 104

ESPI_RESET# 38, 70, 104

Ethernet

GBE0_CTREF 56, 69, 99
GBE0_LINK_ACT# 56, 69, 99
GBE0_LINK_MAX# 69, 99
GBE0_LINK_MAX# 56
GBE0_LINK_MID# 69, 99
GBE0_LINK_MID# 56
GBE0_MDI0- 56, 70, 99
GBE0_MDI0+ 56, 70, 99
GBE0_MDI1- 56, 69, 99
GBE0_MDI1+ 56, 69, 99
GBE0_MDI2- 56, 69, 99
GBE0_MDI2+ 56, 69, 99
GBE0_MDI3- 56, 69, 99
GBE0_MDI3+ 56, 69, 99
GBE0_SDP 56, 69, 99
GBE1_CTREF 57, 69, 103
GBE1_LINK_ACT# 57, 70, 103
GBE1_LINK_MAX# 69, 103
GBE1_LINK_MAX# 57
GBE1_LINK_MID# 69, 103
GBE1_LINK_MID# 57
GBE1_MDI0- 57, 69, 103
GBE1_MDI0+ 57, 69, 103
GBE1_MDI1- 57, 69, 103
GBE1_MDI1+ 57, 69, 103
GBE1_MDI2- 57, 69, 103
GBE1_MDI2+ 57, 69, 103
GBE1_MDI3- 57, 69, 103
GBE1_MDI3+ 57, 69, 103
GBE1_SDP 57, 69, 99

GPIO

GPIO0 ..... 29, 59, 61, 72, 101
GPIO1 ..... 30, 59, 61, 72, 101
GPIO10 ..... 59, 72, 101
GPIO11 ..... 59, 72, 102
GPIO12 ..... 59, 73, 106
GPIO13 ..... 59, 72, 106
GPIO2 ..... 29, 59, 61, 72, 101
GPIO3 ..... 30, 59, 61, 72, 101
GPIO4 ..... 59, 61, 72, 101
GPIO5 ..... 16, 59, 61, 72, 101
GPIO6 ..... 16, 59, 61, 72, 101
GPIO7 ..... 59, 72, 101
GPIO8 ..... 59, 72, 101
GPIO9 ..... 59, 72, 101

I2C

I2C_GP_CK 42, 70, 104
I2C_GP_DAT 42, 70, 104
I2C_LCD_CK 20, 22, 23, 24, 73, 106
I2C_LCD_DAT 20, 22, 23, 24, 73, 106
I2C_PM_CK 63, 72, 102
I2C_PM_DAT 63, 72, 102

Misc

BOOT_SEL0# 64, 65, 72, 102
BOOT_SEL1# 64, 65, 72, 102
BOOT_SEL2# 64, 65, 72, 102
FORCE_RECOV# 64, 73, 106
LID# 63, 73, 106
PWM_OUT 59, 60, 61, 72, 101
RESET_IN# 62, 63, 67, 72, 102
RESET_OUT# 63, 72, 102
RSVD 69, 71, 100, 103, 104, 106
SLEEP# 62, 73, 106
SMB_ALERT# 63, 69, 99
TACHIN 59, 60, 61, 72, 101
TEST# 63, 73, 106
WDT_TIME_OUT# 58, 73, 106

PCIe

PCIE_A_CKREQ# 51, 52, 71, 100
PCIE_A_REFCK- 51, 71, 101
PCIE_A_REFCK+ 51, 71, 101
PCIE_A_RST# 51, 52, 71, 100
PCIE_A_RX- 51, 71, 101
PCIE_A_RX+ 51, 71, 101
PCIE_A_TX- 51, 71, 101
PCIE_A_TX+ 51, 71, 101
PCIE_B_CKREQ# 51, 52, 71, 100
PCIE_B_REFCK- 51, 71, 105
PCIE_B_REFCK+ 51, 71, 105
PCIE_B_RST# 51, 52, 71, 104
PCIE_B_RX- 51, 71, 105
PCIE_B_RX+ 51, 71, 105
PCIE_B_TX- 51, 71, 105
PCIE_B_TX+ 51, 71, 105
PCIE_C_REFCK- 51, 54, 71, 101
PCIE_C_REFCK+ 51, 54, 71, 101
PCIE_C_RST# 51, 52, 54, 71, 104
PCIE_C_RX- 51, 54, 71, 104
PCIE_C_RX+ 51, 54, 71, 104
PCIE_C_TX- 51, 54, 71, 105
PCIE_C_TX+ 51, 54, 71, 105
PCIE_D_RX- 51, 54, 70, 103
PCIE_D_RX+ 51, 54, 70, 103
PCIE_D_TX- 51, 54, 70, 103
PCIE_D_TX+ 51, 54, 69, 103
PCIE_WAKE# 12, 51, 73, 106

Power

BATLOW# 62, 73, 106
CARRIER_PWR_ON 16, 62, 73, 88, 89, 106
CARRIER_STBY# 62, 73, 88, 89, 106
CHARGER_PRSNT# 62, 73, 106
CHARGING# 62, 73, 106

GND..26, 28, 31, 32, 47, 62, 64, 65, 66, 67, 69, 70, 71, 72, 73, 80, 81, 87, 99, 100, 101, 102, 103, 104, 105, 106
POWER_BTN# 63, 72, 102
VDD_IN 17, 62, 66, 73, 87, 89, 102
VDD_RTC 66, 73, 87, 106
VIN_PWR_BAD# 16, 62, 73, 88, 89, 106

QSPI

QSPI_CK 36, 38, 70, 100
QSPI_CS0# 36, 38, 70, 100
QSPI_CS1# 36, 38, 70, 100
QSPI_IO_0 ..... 36, 38, 70, 100
QSPI_IO_1 ..... 36, 38, 70, 100
QSPI_IO_2 ..... 36, 38, 70, 104
QSPI_IO_3 ..... 36, 38, 70, 104

SATA

SATA_ACT# 55, 70, 104
SATA_RX- 70, 100
SATA_RX+ 70, 100
SATA_TX- 70, 100
SATA_TX+ 70, 100

SDIO

SDIO_CD# 34, 70, 99
SDIO_CK 34, 70, 99
SDIO_CMD 34, 70, 99
SDIO_D0 ..... 34, 70, 100
SDIO_D1 ..... 34, 70, 100
SDIO_D2 ..... 34, 70, 100
SDIO_D3 ..... 34, 70, 100
SDIO_PWR_EN 34, 70, 99
SDIO_WP 34, 70, 99

SERDES

MDIO_CLK 53, 54, 70, 104
MDIO_DAT 53, 54, 70, 104
SERDES_0_RX- 53, 54, 70, 103
SERDES_0_RX+ 53, 54, 70, 103
SERDES_0_TX- 53, 54, 70, 103
SERDES_0_TX+ 53, 54, 69, 103
SERDES_1_RX- 53, 54, 71, 104
SERDES_1_RX+ 53, 54, 71, 104
SERDES_1_TX- 53, 54, 71, 105
SERDES_1_TX+ 53, 54, 71, 105

Serial

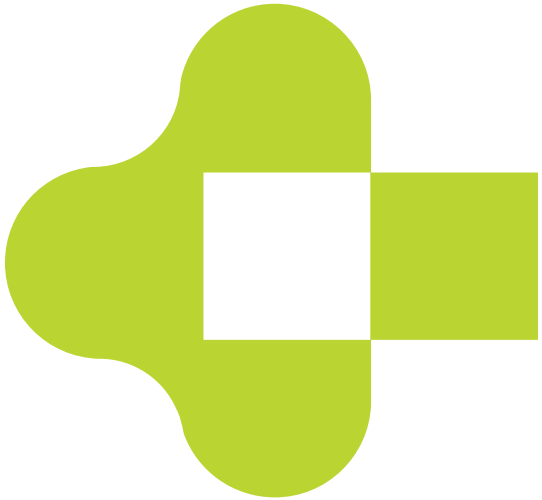
SER0_CTS# 43, 73, 102
SER0_RTS# 43, 72, 102
SER0_RX 43, 72, 102
SER0_TX 43, 72, 102
SER1_RX 43, 73, 102
SER1_TX 43, 73, 102
SER2_CTS# 43, 73, 102
SER2_RTS# 43, 73, 102
SER2_RX 43, 73, 102
SER2_TX 43, 73, 102
SER3_RX 43, 73, 102
SER3_TX 43, 73, 102

SPI

SPI0_CK 35, 70, 100
SPI0_CS0# 35, 70, 100
SPI0_CS1# 35, 70, 99
SPI0_DIN 35, 70, 100
SPI0_DO 35, 70, 100
SPI1_CK 35, 38, 70, 100
SPI1_CS0# 35, 38, 70, 100
SPI1_CS1# 35, 38, 70, 100
SPI1_DIN 35, 38, 70, 100
SPI1_DO 35, 38, 70, 100

USB

USB0- 47, 70, 100
USB0_EN_OC# 47, 70, 100
USB0_OTG_ID 47, 70, 100
USB0_VBUS_DET 47, 70, 100
USB0+ 47, 70, 100
USB1- 47, 71, 100
USB1_EN_OC# 47, 71, 100
USB1+ 47, 71, 100
USB2- 47, 71, 100
USB2_EN_OC# 47, 71, 100
USB2_SSRX- 47, 71, 104
USB2_SSRX+ 47, 71, 104
USB2_SSTX- 47, 71, 104
USB2_SSTX+ 47, 71, 104
USB2+ 47, 71, 100
USB3- 47, 71, 104
USB3_EN_OC# 48, 71, 100
USB3_OTG_ID 48, 72, 105
USB3_SSRX- 47, 71, 104
USB3_SSRX+ 47, 70, 104
USB3_SSTX- 47, 70, 104
USB3_SSTX+ 47, 70, 104
USB3_VBUS_DET 48, 70, 103
USB3+ 47, 71, 104
USB4- 48, 70, 103
USB4_EN_OC# 48, 71, 100
USB4+ 48, 70, 103
USB5- 48, 70, 104
USB5_EN_OC# 48, 70, 104
USB5+ 48, 70, 104



SMARC module