# F75P – 3U CompactPCI<sup>®</sup> PlusIO Safe Railway Computer

- 2x Intel<sup>®</sup> Atom<sup>™</sup> E6xx, 512 MB DDR2 RAM (each) for onboard dual redundancy
- Ix Intel<sup>®</sup> Atom<sup>™</sup> E6xx, 1 GB DDR2 for I/O
- Independent supervisors for each block
- Fail-safe and fail-silent board architecture
- Clustering of two F75P to raise availability
- Event logging
- Certifiable up to SIL 4 (with report from TÜV SÜD)
- SIL 4 certification packages available for hardware and software (QNX<sup>®</sup>)
- Developed according to EN 50129, EN 50128 and IEC 61508
- Full EN 50155 compliance
- -40 to +85°C qualified
- Conformal coating

The F75P is a COTS safe computer with onboard functional safety that unites three CPUs on one 3U CompactPCI<sup>®</sup> PlusIO card. It makes Intel<sup>®</sup> Atom™ E6xx ("E600") performance with dual redundancy extremely compact, mainly targeting railway applications. Two independent Control Processors (CP) with independent DDR2 RAM and Flash and a supervision structure provide safety: with redundant software running on F75P, and, e.g., with the software instances on the two CPs comparing their output, the board becomes a failsilent subsystem, i.e. it can shut down in case of a fatal fault.

Its I/O Processor (IOP) is built up like a classic CompactPCI® CPU board, including DDR2 RAM, front and rear I/O. The front connectors include VGA, two USB 2.0, and two 100-Mbit (Fast) Ethernet channels. At the rear, the board provides another four USB 2.0, two Fast Ethernet ports, one 3-Gbit SATA and one PCI Express® x1 link. These interfaces comply with the standardized pinout of CompactPCI® PlusIO (PICMG 2.30). An onboard mSATA slot makes for scalable, robust mass storage. The intelligent board management controller of the IOP logs events such as reset, overvoltage or undervoltage in a non-volatile FRAM.

The Control (CP) and I/O Processors (IOP) communicate via internal links provided by an FPGA.



The CPs are designed to run a deterministic real-time operating system such as the QNX<sup>®</sup> Neutrino RTOS Safe Kernel or PikeOS. It is also possible to implement diversitary software on both kernels. All three CPUs support Linux and QNX<sup>®</sup>.

The F75P can replace multiprocessing systems with CPU redundancy and I/O by a small-footprint, low-power solution that is flexible for different types of application scenarios. It uses a single +5V supply voltage to allow operation with external power supplies that do not generate +3.3 V.

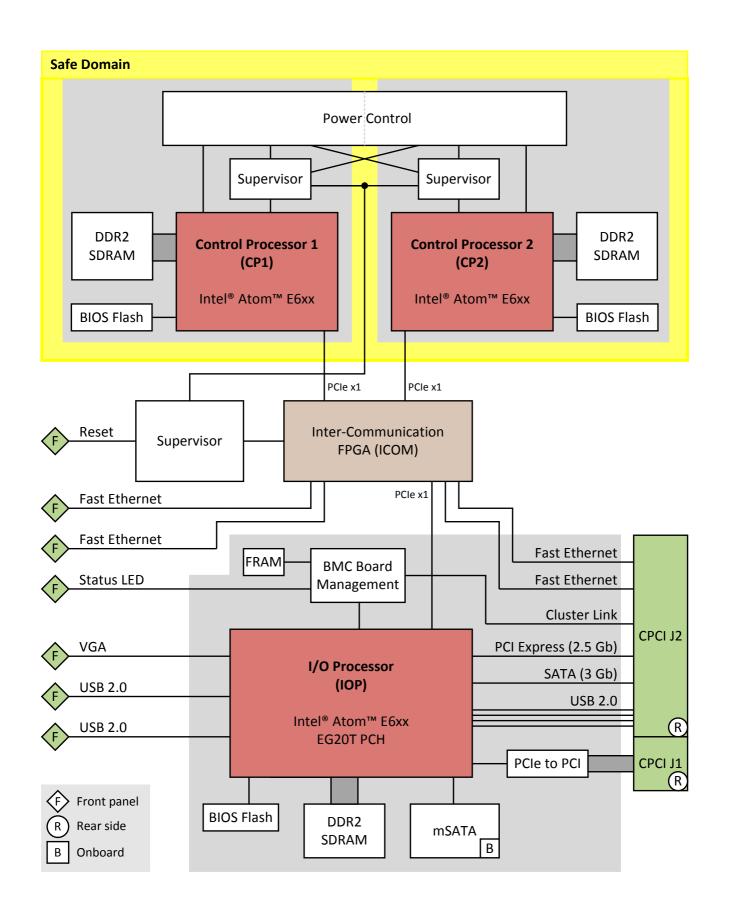
A clustering option is considered as well, to increase system availability: two F75P boards can operate next to each other, and can provide hot or cold stand-by.

F75P-based systems are generally certifiable up to SIL 4. Since the card has no voter of its own, the customer has to add the software that implements and controls functional safety behavior. The safety features such as the CP supervisors are designed to SIL 4 according to EN 50129. A railway certification package including the "safety case" document and a certificate from TÜV SÜD is available.

Its rugged set-up also make the F75P truly rail-ready: with assets like conformal coating and an operating temperature of -40 to +85°C with qualified components, it is fully EN 50155 compliant. A 4-HP version is available with RJ45 Ethernet connectors and a reduced temperature range for system design, while another standard card with 8 HP width provides the necessary space for M12 front connectors and a larger heat sink for -40 to +85°C.



### Diagram



# **Technical Data**

CPU Architecture	<ul> <li>Three onboard processors</li> <li>Two Control Processors (CP)</li> <li>One I/O Processor (IOP)</li> <li>Inter-communication between all three processors via onboard Ethernet or Shared RAM</li> <li>Three identical processor types</li> <li>Intel® Atom™ E6xx Series</li> <li>0.6 GHz to 1.6 GHz processor core frequency</li> <li>Please see Standard Configurations and Options below for options and available standard versions.</li> <li>Main function of CPs</li> <li>Provide a "Safe Domain" on the board, including processors, memory, supervisors and power control</li> <li>Provide flexible implementation options for functional safety requirements</li> <li>Provide support for advanced, certified operating systems up to SIL 4</li> <li>Main function of IOP</li> <li>Provide common I/O and memory facilities</li> <li>Provide a user-friendly software interface and GUI</li> </ul>
Memory (connected to CPs)	<ul> <li>512 KB L2 cache integrated in E6xx for each processor</li> <li>Up to 1 GB SDRAM system memory to each of the Control Processors (CP) <ul> <li>Soldered</li> <li>DDR2</li> <li>800 MHz memory bus frequency (800 MT/s data rate)</li> </ul> </li> <li>2 MB BIOS Flash</li> <li>Please see Standard Configurations and Options below for options and available standard versions.</li> </ul>
Chipset (connected to IOP)	Intel <sup>®</sup> EG20T Platform Controller Hub (PCH)
Memory (connected to IOP)	<ul> <li>512 KB L2 cache integrated in E6xx</li> <li>Up to 2 GB SDRAM system memory <ul> <li>Soldered</li> <li>DDR2</li> <li>800 MHz memory bus frequency (800 MT/s data rate)</li> </ul> </li> <li>2 MB BIOS Flash <ul> <li>8 KB non-volatile FRAM for event logging</li> <li>mSATA disk slot</li> <li>Connected via one SATA channel</li> <li>For IOP boot image and file system</li> </ul> </li> <li>Please see Standard Configurations and Options below for options and available standard versions.</li> </ul>
Mass Storage (connected to IOP)	<ul> <li>Serial ATA (SATA)</li> <li>One port for mSATA onboard devices</li> <li>One port for rear I/O</li> <li>SATA Revision 2.x support</li> <li>Transfer rates up to 300 MB/s (3 Gbit/s)</li> </ul>
Graphics (connected to IOP)	<ul> <li>Integrated in E6xx processor</li> <li>320 or 400 MHz graphics base frequency, depending on processor type</li> <li>Maximum resolution: 1280 x 1024 pixels</li> <li>VGA connector at front panel</li> </ul>

## **Technical Data**

If O (controlled by IOP)USB 20 host ports 		
Two USB 2.0 (Series A)         Rear I/O (PICMG 2.30)         0 One SATA (3 Gb)         Four USB 2.0         Two 10/100Base-T Ethernet         0 One CI Express <sup>*</sup> X1 link         Compatible with PICMC 2.30 CompactPCI <sup>®</sup> PlusIO         - Troto 10/100Base-T Ethernet         0 One PIC Express <sup>*</sup> X1 link         Compatible with PICMC 2.30 CompactPCI <sup>®</sup> PlusIO         - Throto 10/100Base-T Ethernet         0 One PIC Express <sup>*</sup> X1 link         Compatible with PICMC 2.30 CompactPCI <sup>®</sup> PlusIO         - Throto 10/100Base-T Ethernet         0 One PIC Express <sup>*</sup> X1 link         Compatible with PICMC 2.30 CompactPCI <sup>®</sup> PlusIO         - Some pins are used for signals differing from the PICMC 2.30 specification, e.g., for clustering, However, these signals do not destroy or cause any malfunction of a connected 1/O board based on this standard.         Event Logging       = Event history logged in non-volatile FRAM, e.g., reset, overvoltage, undervoltage, excess temperature         25 de entries possible       = Twen Sare generated by board hardware or user application         Cluster Link       = Two F7SP boards can be connected to form a cluster         - Accessible on CompactPCI <sup>®</sup> Lar (/O connector       - Bidirectional, full-duplex, differential interface         Miscellaneous       = Real-time clock with supercapacitor: S6 hours when fully loaded, after 3 years runtime @ 40°C, 24h operation      <	I/O (controlled by IOP)	<ul> <li>Six USB 2.0 host ports</li> <li>Two Series A connectors at front panel</li> <li>Four ports via rear I/O on CompactPCI<sup>®</sup> J2</li> <li>OHCl and EHCl implementation</li> <li>Data rates up to 480 Mbit/s</li> <li>Ethernet</li> <li>Four 10/100Base-T Ethernet channels, via Inter-Communication FPGA</li> <li>Two channels via RJ45 or M12 connectors at front panel, with status LEDs</li> <li>Two channels via rear I/O on CompactPCI<sup>®</sup> J2</li> <li>PCI Express<sup>®</sup></li> <li>One PCI Express<sup>®</sup> x1 link via rear I/O on CompactPCI<sup>®</sup> J2</li> <li>PCIe<sup>®</sup> 1.0a support</li> </ul>
Four USE 2.0         Two 10/100Base-T Ethernet         On PCIE Express* x1 link         Compatible with PICMG 2.30 CompattPCI* PlusIO         IPCI33/PICE2.5/JSKA73/4VUSS2/2ETH100         Some pins are used for signals differing from the PICMG 2.30 specification, e.g., for clustering. However, these signals do not destroy or cause any malfunction of a connected I/O board based on this standard.         Event Logging       E Event history logged in non-volatile FRAM, e.g., reset, overvoltage, undervoltage, excess temperature         2.56 entries possible       Events are generated by board hardware or user application         Cluster Link       Two F75P boards can be connected to form a cluster         Cluster Link       Cluster link interface based on R5422         Accessible on CompactPCI* 2 rear I/O connector       Bidirectional, full-duplex, differential interface         Bidirectional full-duplex, differential interface       Data retention of superapacitor backup connected to I/O Processor         Data retention of superapacitor: S6 hours when fully loaded, after 3 years runtime @ 40°C, 24h operation       Three independent supervisors for Control Processors and Inter-Communication FPGA         CompactPCI* Bus       Compliance with CompactPCI* Core Specification PICMG 2.0 R3.0         System slot       System slot         System slot       System slot         System slot       System slot         System slot       System slot </td <td>Front Connections (Standard)</td> <td>Two USB 2.0 (Series A)</td>	Front Connections (Standard)	Two USB 2.0 (Series A)
= 256 entries possible         = Events are generated by board hardware or user application         Cluster Link       = Two F75P boards can be connected to form a cluster         = Cluster Link (Cluster Link interface based on R5422)       - Accessible on CompactPCI® 12 rear I/O connector         = Bidirectional, full-duplex, differential interface         Miscellaneous       = Real-time clock with supercapacitor backup connected to I/O Processor         = Data retention of supercapacitor: 56 hours when fully loaded, after 3 years runtime @ 40°C, 24h operation         = Three independent supervisors for Control Processors and Inter-Communication FPGA         = Check for overvoltage, undervoltage, excess temperature, internal errors of FPGA and CPUs, CPU and FPGA clock         = Watchdog         = Board Management Controller for I/O Processor         = Status LED at front panel         = Reset button at front panel         = Reset button at front panel         = Board star store with CompactPCI® Core Specification PICMG 2.0 R3.0         = System slot         = 32-bit/33-MHz PCI-to-PCI bridge         * V(U(O): +3.3 V (+5 V tolerant))         Hot insertion and removal without damage         Busless Operation       = Board can be supplied with +5 V only, all other voltages are generated on the board         = Backplane connectors used only for power supply       Electrical Specifications	Rear I/O (PICMG 2.30)	<ul> <li>Four USB 2.0</li> <li>Two 10/100Base-T Ethernet</li> <li>One PCI Express® x1 link</li> <li>Compatible with PICMG 2.30 CompactPCI® PlusIO <ul> <li>1PCI33/1PCIE2.5/1SATA3/4USB2/2ETH100</li> <li>Some pins are used for signals differing from the PICMG 2.30 specification, e.g., for clustering. However, these signals do not destroy or cause any malfunction of a connected I/O board based on this</li> </ul> </li> </ul>
E Cluster link interface based on R5422         Accessible on CompactPCI® J2 rear I/O connector         Bidirectional, full-duplex, differential interface         Miscellaneous         Real-time clock with supercapacitor backup connected to I/O Processor         Data retention of supercapacitor: 56 hours when fully loaded, after 3 years runtime @ 40°C, 24h operation         Three independent supervisors for Control Processors and Inter-Communication FPGA         Check for overvoltage, undervoltage, excess temperature, internal errors of FPGA and CPUs, CPU and FPGA clock         Watchdog         Board Management Controller for I/O Processor         System slot         32-bit/33-MHz PCI-to-PCI bridge         V(I/O): +3.3 V (+5 V tolerant)         Hot insertion and removal without damage         Busless Operation       Board can be supplied with +5 V only, all other voltages are generated on the board         Backplane connectors used only for power supply	Event Logging	<ul> <li>256 entries possible</li> </ul>
Data retention of supercapacitor: 56 hours when fully loaded, after 3 years runtime @ 40°C, 24h operationThree independent supervisors for Control Processors and Inter-Communication FPGACheck for overvoltage, undervoltage, excess temperature, internal errors of FPGA and CPUs, CPU and FPGA clockWatchdogBoard Management Controller for I/O ProcessorStatus LED at front panelReset button at front panelReset button at front panelCompactPCI® BusCompliance with CompactPCI® Core Specification PICMG 2.0 R3.0 System slotSystem slot32-bit/33-MHz PCI-to-PCI bridge V(I/O): +3.3 V (+5 V tolerant) Hot insertion and removal without damageBusless OperationBoard can be supplied with +5 V only, all other voltages are generated on the board Backplane connectors used only for power supplyElectrical SpecificationsSupply voltage/power consumption:	Cluster Link	<ul> <li>Cluster link interface based on RS422</li> <li>Accessible on CompactPCI<sup>®</sup> J2 rear I/O connector</li> </ul>
<ul> <li>System slot</li> <li>32-bit/33-MHz PCI-to-PCI bridge</li> <li>V(I/O): +3.3 V (+5 V tolerant)</li> <li>Hot insertion and removal without damage</li> </ul> Busless Operation <ul> <li>Board can be supplied with +5 V only, all other voltages are generated on the board</li> <li>Backplane connectors used only for power supply</li> </ul> Electrical Specifications <ul> <li>Supply voltage/power consumption:</li> </ul>	Miscellaneous	<ul> <li>Data retention of supercapacitor: 56 hours when fully loaded, after 3 years runtime @ 40°C, 24h operation</li> <li>Three independent supervisors for Control Processors and Inter-Communication FPGA</li> <li>Check for overvoltage, undervoltage, excess temperature, internal errors of FPGA and CPUs, CPU and FPGA clock</li> <li>Watchdog</li> <li>Board Management Controller for I/O Processor</li> <li>Status LED at front panel</li> </ul>
Backplane connectors used only for power supply         Electrical Specifications         Supply voltage/power consumption:	CompactPCI <sup>®</sup> Bus	<ul> <li>System slot</li> <li>32-bit/33-MHz PCI-to-PCI bridge</li> <li>V(I/O): +3.3 V (+5 V tolerant)</li> </ul>
	Busless Operation	
	Electrical Specifications	

## **Technical Data**

Mechanical Specifications	<ul> <li>Dimensions: conforming to CompactPCI<sup>®</sup> specification for 3U boards</li> <li>Front panel: 4 HP or 8 HP with ejector</li> <li>Weight: <ul> <li>4 HP, RJ45 connectors: 402 g (incl. heat sink)</li> <li>8 HP, M12 connectors: 626 g (incl. heat sink)</li> </ul> </li> </ul>
Environmental Specifications	<ul> <li>Temperature range (operation): <ul> <li>-40+50°C in 4 HP version (qualified components)</li> <li>-40+85°C in 8 HP version (qualified components), compliant with EN 50155, class Tx</li> <li>Conditions: airflow 1.5 m/s, typical power dissipation: 22.5 W</li> </ul> </li> <li>Temperature range (storage): -40+85°C</li> <li>Relative humidity (operation): max. 95% non-condensing</li> <li>Relative humidity (storage): max. 95% non-condensing</li> <li>Altitude: -300 m to +3000 m</li> <li>Vibration (function): 1 m/s<sup>2</sup>, 5 Hz - 150 Hz (EN 50155 (12.2.11) / EN 61373)</li> <li>Vibration (lifetime): 7.9 m/s<sup>2</sup>, 5 Hz - 150 Hz (EN 50155 (12.2.11) / EN 61373)</li> <li>Shock: 50 m/s<sup>2</sup>, 30 ms (EN 50155 (12.2.11) / EN 61373)</li> <li>Conformal coating (standard)</li> </ul>
MTBF	277 975 h @ 40°C according to IEC/TR 62380 (RDF 2000)
Safety	<ul> <li>Functional Safety</li> <li>Certifiable up to SIL 4 according to EN 50129 ("safety case" document and certificate from TÜV SÜD available)</li> <li>Hazard rate for safety functions &lt;= 1E-9 / h</li> <li>Control Processors configured for deterministic behavior, e.g., Hyper-Threading disabled, speed-step disabled, BIOS interrupts disabled</li> <li>Board maintains safe state after a failure (factory configuration)</li> <li>Flammability</li> <li>PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers</li> </ul>
EMC Conformity	<ul> <li>When integrated into an EMC protected rack</li> <li>EN 50121-3-2 (tables 5 and 6) / EN 55011 (radio disturbance)</li> <li>EN 50121-3-2 (table 9) / IEC 61000-4-6 (ESD)</li> <li>EN 50121-3-2 (table 9) / IEC 61000-4-3 (electromagnetic field immunity)</li> <li>EN 50121-3-2 (table 8) / IEC 61000-4-4 (burst)</li> <li>EN 50121-3-2 (table 8) / IEC 61000-4-6 (conducted disturbances)</li> </ul>
BIOS	■ InsydeH2O <sup>TM</sup> UEFI Framework
Software Support	<ul> <li>I/O Processor</li> <li>Linux (in preparation)</li> <li>QNX<sup>®</sup> (in preparation)</li> <li>VxWorks<sup>®</sup> (on request)</li> <li>Control Processors</li> <li>QNX<sup>®</sup> (with or without Safe Kernel) (in preparation)</li> <li>PikeOS</li> <li>Linux (in preparation)</li> <li>VxWorks<sup>®</sup> (on request)</li> <li>VxWorks<sup>®</sup>/Cert (on request)</li> <li>For more information on supported operating system versions and drivers see Downloads.</li> </ul>

# **Configuration & Options**

#### **Standard Configurations**

Article No.	СРИ Туре	System RAM	Ethernet connectors	Front Panel	Conformal Coating	Operating Temperature
02F075P00	3x E680T, 1.6 GHz	CPs: 512 MB each, IOP: 1 GB	RJ45	4 HP	Yes	-40+50°C qualified
02F075P01	3x E680T, 1.6 GHz	CPs: 512 MB each, IOP: 1 GB	M12 (right)	8 HP	Yes	-40+85°C qualified
Options						
СРИ		<ul> <li>Intel<sup>®</sup> Atom<sup>™</sup> E620T, 0.6 GHz, 320 MHz graphics frequency, 3.3 W TDP (estimated)</li> <li>Intel<sup>®</sup> Atom<sup>™</sup> E640T, 1.1 GHz, 320 MHz graphics frequency, 3.6 W TDP</li> <li>Intel<sup>®</sup> Atom<sup>™</sup> E660T, 1.3 GHz, 400 MHz graphics frequency, 3.6 W TDP</li> <li>Intel<sup>®</sup> Atom<sup>™</sup> E680T, 1.6 GHz, 400 MHz graphics frequency, 4.5 W TDP (estimated)</li> </ul>				
Memory		<ul> <li>System RAM</li> <li>512 MB or 1 GB for each Control Processor</li> <li>1 GB or 2 GB for I/O Processor</li> <li>mSATA disk</li> <li>0 MB up to maximum available</li> </ul>				
I/O		<ul> <li>Ethernet</li> <li>RJ45 or M12 connectors</li> <li>M12 connectors need a second front-panel slot (8 HP total width) and can be placed to the left or right side of the CPU PCB.</li> </ul>				
Operating Temper		<ul> <li>-40+50°C (4 HP)</li> <li>-40+85°C (8 HP, with larger heat sink)</li> <li>Depends on heat sink configuration</li> </ul>				
Coating		With or without conformal coating				
Cooling Concept		Also available with conduction cooling in MEN CCA frame				
Restart Option	1	Board can be configured to restart automatically after entering safe state (by factory configuration)			onfiguration)	
Software Support <ul> <li>VxWorks® for I/O / Control Processors (on request)</li> <li>VxWorks®/Cert for Control Processors (on request)</li> </ul>						

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

# **Ordering Information**

Standard F75P Models	02F075P00	3x Intel <sup>®</sup> Atom™ E680T (1.6 GHz), 2x 512 MB, 1x 1 GB DDR2 DRAM, RJ45 ETH connectors, 4 HP, -40+50°C with qualified components, conformal coating			
	02F075P01	3x Intel <sup>®</sup> Atom <sup>™</sup> E680T (1.6 GHz), 2x 512 MB, 1x 1 GB DDR2 DRAM, 8 HP, Ethernet on the right by 2x M12, -40+85°C with qualified components, conformal coating			
Related Hardware	08CT12-00	CompactPCI <sup>®</sup> PlusIO rear transition module 3U/80mm, 2 Ethernet, 4 USB, 4 SATA, 4 PCIe <sup>®</sup> x1, -40°C+85°C qualified			
Memory	0751-0051	SSD mSATA, 8 GB, -40+85°C			
Certification Packages	23F075P00	SIL 4 railway certification package according to EN 5012x for F75P, including:			
		<ul> <li>Safety User Guide including the safety-relevant application requirements, a detailed description of the hardware and instructions for appropriate operation.</li> <li>Safety Case describing the concepts for reaching functional safety as well as all safety and quality-relevant processes and measures to meet the SIL 4 requirements.</li> <li>Assessment report and SIL 4 certificate from TÜV SÜD (German Technical Inspection Agency).</li> <li>40 hours support</li> </ul>			
		Please contact us to get more information about the certification package and to request a copy of the documents.			
	For more information on the F75P certification packages, see this introductory overview presentation (PDF).				
	23F075P40	SIL 4 railway certification package according to EN 5012x for F75P with QNX $^{\circ}$ , including:			
		Safety User Guide including the safety-relevant application requirements, a detailed description of the F75P/QNX <sup>®</sup> hardware/software package and instructions for appropriate operation of the HW/SW package. Safety Case describing the concepts for reaching functional safety as well as all safety and quality-relevant processes and measures to meet the SIL 4 requirements. Assessment report and SIL 4 certificate from TÜV SÜD (German Technical Inspection Agency) covering the F75P/QNX <sup>®</sup> hardware/software bundle. 90 hours support			
		Please contact us to get more information about the certification package and to request a copy of the documents.			
Systems & Card Cages	0701-0046	CompactPCI <sup>®</sup> 19" 4U/24HP desktop system for 3U cards, 3-slot 3U CompactPCI <sup>®</sup> backplane, system slot right, 1U fan tray with 1 fan, 8 HP space for 1 pluggable PSU			
	0701-0056	CompactPCI® 19" 4U/84HP rack-mount enclosure for 3U cards (vertical), 4+4-slot 3U CompactPCI® / CompactPCI® Serial hybrid backplane, prepared for rear I/O, 250W power supply wide range 90264VAC on rear, 1U fan tray with 2 fans included, 0+60°C			
Software: Linux	This product is de	signed to work under Linux. See below for all available separate software packages.			
	13MD05-90	MDIS5 System (and Device Driver) Package (MEN) for Linux. This software package includes most standard device drivers available from MEN.			
	13MM02-90	Linux driver (MEN) for RX8581 real-time clock for CB70C, F75P, MM2, SC24, SC25, BC50M, BC50I, BL50W, BL50S, BL70W and BL70S. Please note that this driver is already included in upstream Linux kernels starting from 3.14!			
	13Y026-90	Linux demo application (MEN) for F75P			
	13Z077-91	Linux Ethernet driver (MEN) for F75P			

# **Ordering Information**

Software: QNX®		esigned to work under QNX <sup>®</sup> . For details regarding supported/unsupported board functions				
	please refer to the	please refer to the corresponding software data sheets.				
	10F075P40	Safe QNX <sup>®</sup> BSP (MEN) for F75P control processors 1 and 2; file is delivered via email upon order				
	10F075P45	QNX® BSP (MEN) for F75P I/O processor; file is delivered via email upon order				
Software: PikeOS	This product is designed to work under PikeOS by SYSGO. The PikeOS BSP is certifiable according to EN 50128 SIL 4 together with the F75P. PikeOS is a real-time operating system for use in safety and mission-critical systems. For more information please contact www.sysgo.com.					
For operating systems not mention	ed here contact ME	EN sales.				
Documentation	Compare Chart 3U CompactPCI <sup>®</sup> Serial CPU and I/O cards » Download					
	Compare Chart safe computers from MEN » Download					
	Compare Chart 3	Compare Chart 3U CompactPCI <sup>®</sup> / PlusIO CPU cards » Download				
	Compare Chart 3	U CompactPCI® / PlusIO peripheral cards » Download				
	21F075P90	F75P Linux User Guide				
	23F075P00	SIL 4 railway certification package according to EN 5012x for F75P, including:				
		<ul> <li>Safety User Guide including the safety-relevant application requirements, a detailed description of the hardware and instructions for appropriate operation.</li> <li>Safety Case describing the concepts for reaching functional safety as well as all safety and quality-relevant processes and measures to meet the SIL 4 requirements.</li> <li>Assessment report and SIL 4 certificate from TÜV SÜD (German Technical Inspection Agency).</li> <li>40 hours support</li> </ul>				
		Please contact us to get more information about the certification package and to request a copy of the documents.				
	For more information on the F75P certification packages, see this introductory overview presentation (PDF).					
	23F075P40	SIL 4 railway certification package according to EN 5012x for F75P with QNX <sup>®</sup> , including:				
		Safety User Guide including the safety-relevant application requirements, a detailed description of the F75P/QNX <sup>®</sup> hardware/software package and instructions for appropriate operation of the HW/SW package. Safety Case describing the concepts for reaching functional safety as well as all safety and quality-relevant processes and measures to meet the SIL 4 requirements. Assessment report and SIL 4 certificate from TÜV SÜD (German Technical Inspection Agency) covering the F75P/QNX <sup>®</sup> hardware/software bundle. 90 hours support				
		Please contact us to get more information about the certification package and to request a copy of the documents.				
	our white paper F	tion on the architecture of safe computer systems based on 3U CompactPCI®, please read Railway Computer 3.0: An Innovative Board Design Could Revolutionize The Market, h and German. » Download				

### **Contact Information**

#### Germany

MEN Mikro Elektronik GmbH Neuwieder Straße 3-7 90411 Nuremberg Phone +49-911-99 33 5-0 Fax +49-911-99 33 5-901

info@men.de www.men.de

#### France

MEN Mikro Elektronik SAS 18, rue René Cassin ZA de la Châtelaine 74240 Gaillard Phone +33 (0) 450-955-312 Fax +33 (0) 450-955-211

info@men-france.fr www.men-france.fr USA

MEN Micro Inc. 860 Penllyn Blue Bell Pike Blue Bell, PA 19422 Phone (215) 542-9575 Fax (215) 542-9577

www.men.de/products/02F075P.html

sales@menmicro.com www.menmicro.com

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